TB071

Converting from Motorola® HC08 to Microchip Assembler: A Quick Reference

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When migrating assembly language programs from one family of microcontrollers to another, the first question is almost always: “What’s the equivalent opcode?” Some operations, like addition and subtraction, are self-evident and practically universal. Other instructions may have some subtle changes in syntax or spelling that make direct conversions a bit trickier. Occasionally, some instructions simply don’t have a direct equivalent in the target set, or an equivalent exists but is explained in different terms.

To help simplify the conversion process, Microchip has compiled a table of the instruction set of the Motorola HC08 8-bit microcontroller family, and their equivalents in the PICmicro® instruction sets (Table 1). It is organized alphabetically by the Motorola instruction mnemonic in the first column, followed by the common description of the operation and the closest equivalent opcode or opcode sequence in the Microchip PIC16 and PIC18 instruction sets. In addition, the size of the instructions (in words or bytes, as appropriate) and the number of clock cycles required for execution are listed for each entry.

There are some instructions in the Microchip architecture that do not have exact equivalents in the HC08 architecture. For the convenience of users more familiar with Motorola instructions, these are listed separately in Table 2. They are organized alphabetically by the PIC18 mnemonic in the first column, followed by the PIC16 equivalent, the closest Motorola HC08 equivalent or equivalent sequence, and the common description. Again, information on the instruction size and execution time is provided.

It is important to remember that this reference list is only a starting point for code conversion. There are several considerations to keep in mind when moving code from 8-bit Motorola devices to Microchip devices:

1. The basic processor architecture is significantly different. The Motorola HC08 processor core is a von Neumann machine which places data and program memory in the same flat memory space and accesses all information through a single bus. In contrast, all Microchip processor cores are Harvard machines which use separate data and program memory spaces and two separate busses.
2. Both Motorola and Microchip use a data memory that is 8 bits wide. With their core architecture, Motorola HC08 devices are also limited to 8-bit wide program memories as well. Microchip PICmicro devices, on the other hand, have program memories that are either 14 bits or 16 bits wide (PIC16 and PIC18 families, respectively).
3. The smaller program memory width in Motorola devices results in greater variance in the size of instructions, from one to four bytes (depending on the operand requirements of the instruction). In contrast, Microchip instructions are mostly single word (two bytes) with a small amount of two-word instructions. In general, the first byte of the opcode represents the instruction, while the second byte represents the data or address payload.
4. The Motorola HC08 instruction set incorporates 12 distinct Addressing modes for its memory space, including 5 Indexed modes and 3 Relative modes. The Indexed modes offer several combinations of 8-bit and 16-bit offsets plus post-operation incrementing. Additionally, many instructions are able to use several different Addressing modes.

   The Microchip core instruction set uses three basic Addressing modes (Immediate, Direct and Indirect). Each instruction is associated with one, and only one, Addressing mode. Only core arithmetic and logic operations have immediate and indirect addressing variants; each version is a distinct instruction with its own distinct mnemonic. The address information is always embedded as part of the instruction word itself.

   For instructions that use indirect addressing, PIC18 devices have implemented File Select Registers (FSRs). These enable a form of indirect addressing that is functionally similar to indexed addressing. The FSRs also provide the options for pre-increment, post-increment, post-decrement, and the use of 8-bit offsets.

All of these differences can significantly change the way that both data and logical program structures are implemented. This is particularly true when indexed and indirect addressing methods are used to direct code execution. Users are encouraged to review existing Microchip application notes for the appropriate family to get an idea of how different applications are implemented.

TABLE 1: MOTOROLA HC08 INSTRUCTIONS AND THEIR MICROCHIP EQUIVALENTS

Motorola HC08			Operation	Microchip					
				PIC16			PIC18		
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
ADC	1-4	2-5	Add with Carry	BTFSC STATUS,C INCF M,F ADDWF M,F	3	3	ADDWFC M,F	2	1
ADD	1-4	2-5	Add without Carry(1)	ADDWF M,F	1	1	ADDWF M,F	2	1
	2	2	ADD Literal with WREG(2)	ADDLW	1	1	ADDLW	2	1
AIS	2	2	Add Immediate Value to Stack Pointer	No equivalent instruction					
AIX	2	2	Add Immediate Value to Stack Pointer	No equivalent instruction					
AND	1-4	2-5	Logical AND(1)	ANDWF M,F	1	1	ANDWF M,F	2	1
	2	2	Logical AND Literal with WREG(2)	ANDLW	1	1	ANDLW	2	1
ASL	1-3	1-6	Arithmetic Shift Left	BCF STATUS,C RLF M,F	2	2	BCF STATUS,C RLCF M,F	4	2
ASR	1-3	1-6	Arithmetic Shift Right	BCF STATUS,C BTFSC M,7 BSF STATUS,C RRF M,F	4	4	BCF STATUS,C BTFSC M,7 BSF STATUS,C RRCF M,F	8	4
BCC	2	3	Branch if Carry Bit Clear	BTFSS STATUS,C GOTO addr	2	3	BNC rel	2	1
BCLR n	2	5	Clear Bit n in Memory	BCF M,n	1	1	BCF M,n	2	1
BCS	2	3	Branch if Carry Bit Set	BTFSC STATUS,C GOTO addr	2	3	BC rel	2	2
BEQ	2	3	Branch if Equal	BTFSC STATUS,Z GOTO addr	2	3	BZ rel	2	2
BGE	2	3	Branch if Greater Than or Equal To	No Equivalent PIC16 instruction			CPFSLT BRA rel	4	2-3

Legend: For Microchip mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in Motorola architecture).

Note 1: Direct or indirect addressing version of instruction depending on the registers selected by M and F; equivalent to Direct, Extended or Indexed Addressing modes in Motorola architecture.

2: Immediate addressing version of instruction; equivalent to Immediate Addressing mode in Motorola architecture.

3: Reference routines are the 8-bit fixed-point Multiply and Divide routines specified in the Microchip application note AN617, “Fixed Point Routines” (DS00617).

4: Reference routine for PIC18 devices is the 8-bit fixed-point Divide routine provided with the Microchip MPLAB® C18 C compiler.

TABLE 1: MOTOROLA HC08 INSTRUCTIONS AND THEIR MICROCHIP EQUIVALENTS (CONTINUED)

Motorola HC08			Operation	Microchip					
				PIC16			PIC18		
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
BGT	2	3	Branch if Greater Than	No Equivalent PIC16 instruction			BTFSS STATUS,N BNOV rel BTFSS STATUS,OV BNN rel	8	6-8
BHCC	2	3	Branch if Half Carry Bit Clear	BTFSS STATUS,DC GOTO addr	2	3	BTFSS STATUS,DC BRA rel	4	3
BHCS	2	3	Branch if Half Carry Bit Set	BTFSC STATUS,DC GOTO addr	2	3	BTFSC STATUS,DC BRA rel	4	3
BHI	2	3	Branch if Higher	BTFSC STATUS,C GOTO addr BTFSC STATUS,Z GOTO addr	4	3-5	BC rel BZ rel	4	2 or 4
BHS	2	3	Branch if Higher or Same	BTFSS STATUS,C GOTO addr	2	3	BNC rel	2	2
BHI	2	3	Branch if IRQ Pin High	BTFSC PORTx,<pin> GOTO addr	2	3	BTFSC PORTx,<pin> BRA rel	4	3
BIL	2	3	Branch if IRQ Pin Low	BTFSS PORTx,<pin> GOTO addr	2	3	BTFSS PORTx,<pin> BRA rel	4	3
BIT	1-4	2-5	Bit Test	MOVLW <mask> ANDWF M,W	2	2	MOVLW <mask> ANDWF M,W	4	2
BLE	2	3	Branch if Less Than or Equal To	No equivalent PIC16 instruction			CPFSGT F BRA rel F	4	2-3
BLO	2	3	Branch if Lower	BTFSC STATUS,C GOTO addr	2	3	BNC rel	2	1

Legend: For Microchip mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in Motorola architecture).

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Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
BLS	2	3	Branch if Lower or Same	BTFSC STATUS,C GOTO addr BTFSC STATUS,Z GOTO addr	4	3-5	BC rel BZ rel	4	2 or 4
BLT	2	3	Branch if Less Than	No equivalent PIC16 instruction			BTFSS STATUS,N BOV rel BTFSS STATUS,OV BTFSS STATUS,OV BN rel	8	6-8
BMC	2	3	Branch if Interrupt Mask Clear	BTFSS INTCON,GIE GOTO addr	2	3	BTFSS INTCON,GIE BRA rel	4	3
BMI	2	3	Branch if Minus	BTFSC M,7 GOTO addr	2	3	BN rel	2	2
BMS	2	3	Branch if Interrupt Mask Set	BTFSC INTCON,GIE GOTO addr	2	3	BTFSC INTCON,GIE BRA rel	4	3
BNE	2	3	Branch if Not Equal	BTFSS STATUS,Z GOTO addr	2	3	BNZ rel	2	2
BPL	2	3	Branch if Plus	BTFSS M,7 GOTO addr	2	3	BNN rel	2	2
BRA	2	3	Branch Always	GOTO addr	1	2	BRA rel	2	2
BRCLR n	3	5	Branch if Bit n in Memory Clear	BTFSS M,n GOTO addr	2	3	BTFSS M,n BRA rel	4	3
BRN	2	3	Branch Never	GOTO $	1	2	BRA $	2	2
BRSET n	3	5	Branch if Bit n in Memory Set	BTFSC M,n GOTO addr	2	3	BTFSC M,n BRA rel	4	3

Legend: For Microchip mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in Motorola architecture).

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TABLE 1: MOTOROLA HC08 INSTRUCTIONS AND THEIR MICROCHIP EQUIVALENTS (CONTINUED)

Motorola HC08			Operation	Microchip				
				PIC16			PIC18	
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
BSET n	2	5	Set Bit n in Memory	BSF M,n	1	1	BSF M,n	2	1
BSR	2	5	Branch to Subroutine	CALL addr	1	2	RCALL rel	2	2
CBEQ	2-4	4-6	Compare and Branch if Equal	SUBWF M,W BTFSC STATUS,Z GOTO addr	3	4	CMPSEQ	2	2
CLC	1	1	Clear Carry Bit	BCF STATUS,C	1	1	BCF STATUS,C	2	1
CLI	1	1	Clear Interrupt Mask Bit	BCF INTCON,GIE	1	1	BCF INTCON,GIE	2	1
CLR	1-3	1-6	Clear	CLRF M	1	1	CLRF M	2	1
CMP	1-4	2-5	Compare Accumulator with Memory	SUBWF M,W	1	1	SUBWF M,W	2	1
COM	1-3	1-6	Complement (One's Complement)	COMF M,F	1	1	COMF M,F	2	1
CPHX	2-3	3-6	Compare Index Register with Memory	No equivalent instruction					
CPX	1-4	2-5	Compare X (Index Register) with Memory	MOVF M,W SUBWF FSR,W	2	2	MOVF M,W SUBWF FSR0L,W	4	2
DAA	1	1	Decimal Adjust Accumulator	ADDLW 0x06 BTFSS STATUS,DC GOTO $+3 ADDLW 0x10 GOTO $+2 ADDLW 0xFA ADDLW 0x60 BTFSS STATUS,DC ADDLW 0xA0	9	10	DAW M,F	2	1

Legend: For Microchip mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in Motorola architecture).

Note 1: Direct or indirect addressing version of instruction depending on the registers selected by M and F; equivalent to Direct, Extended or Indexed Addressing modes in Motorola architecture.

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4: Reference routine for PIC18 devices is the 8-bit fixed-point Divide routine provided with the Microchip MPLAB® C18 C compiler.

TABLE 1: MOTOROLA HC08 INSTRUCTIONS AND THEIR MICROCHIP EQUIVALENTS (CONTINUED)

Motorola HC08			Operation	Microchip					
				PIC16			PIC18		
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
DBNZ	2-4	4-8	Decrement and Branch if Not Zero	DECF M,F BTFSS STATUS,Z GOTO addr	3	4	DCFSNZ M,F BRA rel	4	3
DEC	1-3	1-6	Decrement	DECF M,F	1	1	DECF M,F	2	1
DIV	1	6	Divide	(Divide Routine)(3)	41	269	(Divide Routine)(4)	50	55
EOR	1-4	2-5	Exclusive-OR Memory with Accumulator(1)	XORWF M,F	1	1	XORWF M,F	2	1
	2	2	Exclusive-OR Literal with WREG(2)	XORLW	1	1	XORLW	2	1
INC	1-3	1-6	Increment	INCF M,F	1	1	INCF M,F	2	1
JMP	1-3	3-4	Jump	GOTO addr	1	2	BRA addr	2	2
JSR	1-3	5-6	Jump to Subroutine	CALL rel	1	2	RCALL rel	2	2
LDA	1-4	2-5	Load Accumulator from Memory	MOVF M,W	1	1	MOVF M,W	2	1
	2	2	Move Literal to WREG(2)	MOVLW	1	1	MOVLW	2	1
LDHX	2-4	3-6	Load Index Register from Memory	No equivalent PIC16 instruction			LFSR	4	2
LDX	1-4	2-5	Load X (Index Register Low) from Memory	MOVF M,W MOVWF FSR	2	2	MOVFF FSR0L,M	4	2
LSL	1-3	1-6	Logical Shift Left	BCF STATUS,C RLF M,F	2	2	BCF STATUS,C RLF M,F	4	2
LSR	1-3	1-6	Logical Shift Right	BCF STATUS,C RRF M,F	2	2	BCF STATUS,C RRF M,F	4	2
MOV	2-3	4-5	Move	MOVF M,W MOVWF N	2	2	MOVFF N,M	4	2
MUL	1	5	Unsigned Multiply	(Multiply Routine)(3)	21	74	MULWF M,F	2	1

Legend: For Microchip mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in Motorola architecture).

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4: Reference routine for PIC18 devices is the 8-bit fixed-point Divide routine provided with the Microchip MPLAB® C18 C compiler.

TABLE 1: MOTOROLA HC08 INSTRUCTIONS AND THEIR MICROCHIP EQUIVALENTS (CONTINUED)

Motorola HC08			Operation	Microchip					
				PIC16			PIC18		
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
NEG	1-3	1-6	Negate (Two's Complement)	COMF M,F INCF M,F	2	2	NEGF M,F	2	1
NOP	1	1	No Operation	NOP	1	1	NOP	2	1
NSA	1	1	Nibble Swap Accumulator	SWAPF M,F	1	1	SWAPF M,F	2	1
ORA	1-4	2-5	Inclusive-OR Accumulator and Memory(1)	IORWF M,F	1	1	IORWF M,F	2	1
	2	2	Inclusive-OR Literal with WREG(2)	IORLW	1	1	IORLW	2	1
PSHA	1	2	Push Accumulator onto Stack	No equivalent PIC16 instruction			PUSH	2	1
PSHH	1	2	Push H (Index Register High) onto Stack	No equivalent PIC16 instruction			PUSH	2	1
PSHX	1	2	Push X (Index Register Low) onto Stack	No equivalent PIC16 instruction			PUSH	2	1
PULA	1	3	Pull Accumulator from Stack	No equivalent PIC16 instruction			POP	2	1
PULH	1	3	Pull H (Index Register High) from Stack	No equivalent PIC16 instruction			POP	2	1
PULX	1	3	Pull X (Index Register Low) from Stack	No equivalent PIC16 instruction			POP	2	1
ROL	1-3	1-6	Rotate Left through Carry	RLF M,F	1	1	RLCF M,F	2	1
ROR	1-3	1-6	Rotate Right through Carry	RRF M,F	1	1	RRCF M,F	2	1
RSP	1	1	Reset Stack Pointer	No equivalent instruction					
RTI	1	9	Return from Interrupt	RETFIE	1	2	RETFIE	2	2
RTS	1	6	Return from Subroutine	RETURN	1	2	RETURN	2	2
SBC	1-4	2-5	Subtract with Carry	BTFSS STATUS,C INCF M,F SUBWF M,F	3	3	SUBFWB M,F	2	1
SEC	1	1	Set Carry Bit	BSF STATUS,C	1	1	BSF STATUS,C	2	1
SEI	1	1	Set Interrupt Mask Bit	BSF INTCON,GIE	1	1	BSF INTCON,GIE	2	1
STA	1-4	2-5	Store Accumulator in Memory	MOVWF M	1	1	MOVWF M	2	1

Legend: For Microchip mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in Motorola architecture).

Note 1: Direct or indirect addressing version of instruction depending on the registers selected by M and F; equivalent to Direct, Extended or Indexed Addressing modes in Motorola architecture.

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TABLE 1: MOTOROLA HC08 INSTRUCTIONS AND THEIR MICROCHIP EQUIVALENTS (CONTINUED)

Motorola HC08			Operation	Microchip					
				PIC16			PIC18		
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
STHX	2-3	4-5	Store Index Register	MOVF FSR,W MOVWF M	2	2	MOVFF M,FSR0L MOVFF M+1,FSR0H	8	4
STOP	1	2	Enable IRQ Pin, Stop Processing	SLEEP	1	1	SLEEP	2	1
STX	1-4	2-5	Store X (Index Register Low) in Memory	MOVF FSR,W MOVWF M	2	1	MOVFF M,FSR0	4	2
SUB	1-4	2-5	Subtract(1)	SUBWF M,F	1	1	SUBWF M,F	2	1
	2	2	Subtract Literal from WREG(2)	SUBLW	1	1	SUBLW	2	1
SWI	1	11	Software Interrupt	CALL 0x0004	1	2	CALL 0x0008	2	2
TAP	1	1	Transfer Accumulator to CCR	MOVWF STATUS	1	1	MOVWF STATUS	2	1
TAX	1	1	Transfer Accumulator to X (Index Register Low)	MOVWF FSR	1	1	MOVWF FSR0L	2	1
TPA	1	1	Transfer CCR to Accumulator	MOVF STATUS,W	1	1	MOVF STATUS,W	2	1
TST	1-3	1-5	Test for Negative or Zero	MOVLW O SUBWF M,W	2	2	CLRF WREG SUBWF M,W	4	2
TSX	1	2	Transfer Stack Pointer to Index Register	No equivalent instruction					
TXA	1	1	Transfer X (Index Register Low) to Accumulator	MOVF FSR,W	1	1	MOVF FSR0L,W	2	1
TXS	1	2	Transfer Index Register to Stack Pointer	No equivalent instruction					
WAIT	1	2	Enable Interrupts, Stop Processor	SLEEP	1	1	SLEEP	2	1

Legend: For Microchip mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in Motorola architecture).

Note 1: Direct or indirect addressing version of instruction depending on the registers selected by M and F; equivalent to Direct, Extended or Indexed Addressing modes in Motorola architecture.

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TABLE 2: MICROCHIP PIC18 INSTRUCTIONS WITHOUT EXACT EQUIVALENTS IN THE MOTOROLA HC08 FAMILY

Microchip						Motorola HC08 Equivalent			Operation
PIC18			PIC16			Instruction(s)	Bytes	Cycles	
Instruction	Bytes	Cycles	Instruction(s)	Words	Cycles				
BTG	2	1	MOVLW # XORWF M,F	2	2	LDA M EOR # STA M	6	8	Bit Toggle File
CLRWDT	2	1	CLRWDT	1	1	No equivalent instruction			Clear Watchdog Timer
DECFSZ	2	2	DECFSZ	1	2	DEC M BNE	4	8	Decrement File, Skip if Zero
INCFSNZ	2	2	INCF M,F BTFSC STATUS,Z	2	3	INC M BEQ	4	8	Increment File, Skip if Not Zero
INCFSZ	2	2	INCFSZ	1	2	INC M BNE	4	8	Increment File, Skip if Zero
MOVLB	2	1	No equivalent instruction			No equivalent instruction			Move Literal to BSR
MULLW	2	1	(Multiply Routine)(1)	21	74	LDX MUL	3	7	Multiply Literal with WREG
RETLW	2	2	RETLW	1	2	LDA # RTS	3	8	Return with Literal in WREG
RLNCF	2	1	RLF M,W RLF M,F	2	2	LSL M BCC rel BSET 0,M	6	13	Rotate Left File, No Carry
RRNCF	2	1	RRF M,W RRF M,F	2	2	LSR M BCC rel BSET 7,M	6	13	Rotate Right File, No Carry
SETF	2	1	MOVLW 0xFF MOVWF M	2	2	LDA #FF STA M	4	5	Set File to all ‘1’s
SUBWFB	2	1	BTFSS STATUS,C INCF M,F SUBWF M,F	3	3	STA N LDA M SBC	6	9	Subtract File from WREG with Borrow
TBLRD	2	2	No equivalent instruction			Similar to indexed MOV instruction			Table Read
TBLWT	2	2	No equivalent instruction			Similar to indexed MOV instruction			Table Write

Legend: For Microchip mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in Motorola architecture).

Note 1: Reference routine is the 8-bit fixed-point Multiply specified in the Microchip application note AN617, “Fixed Point Routines” (DS00617).

NOTES:

Note the following details of the code protection feature on Microchip devices:

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