Section 26. Comparator

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33E/PIC24E devices.

Please consult the note at the beginning of the **"Comparator"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

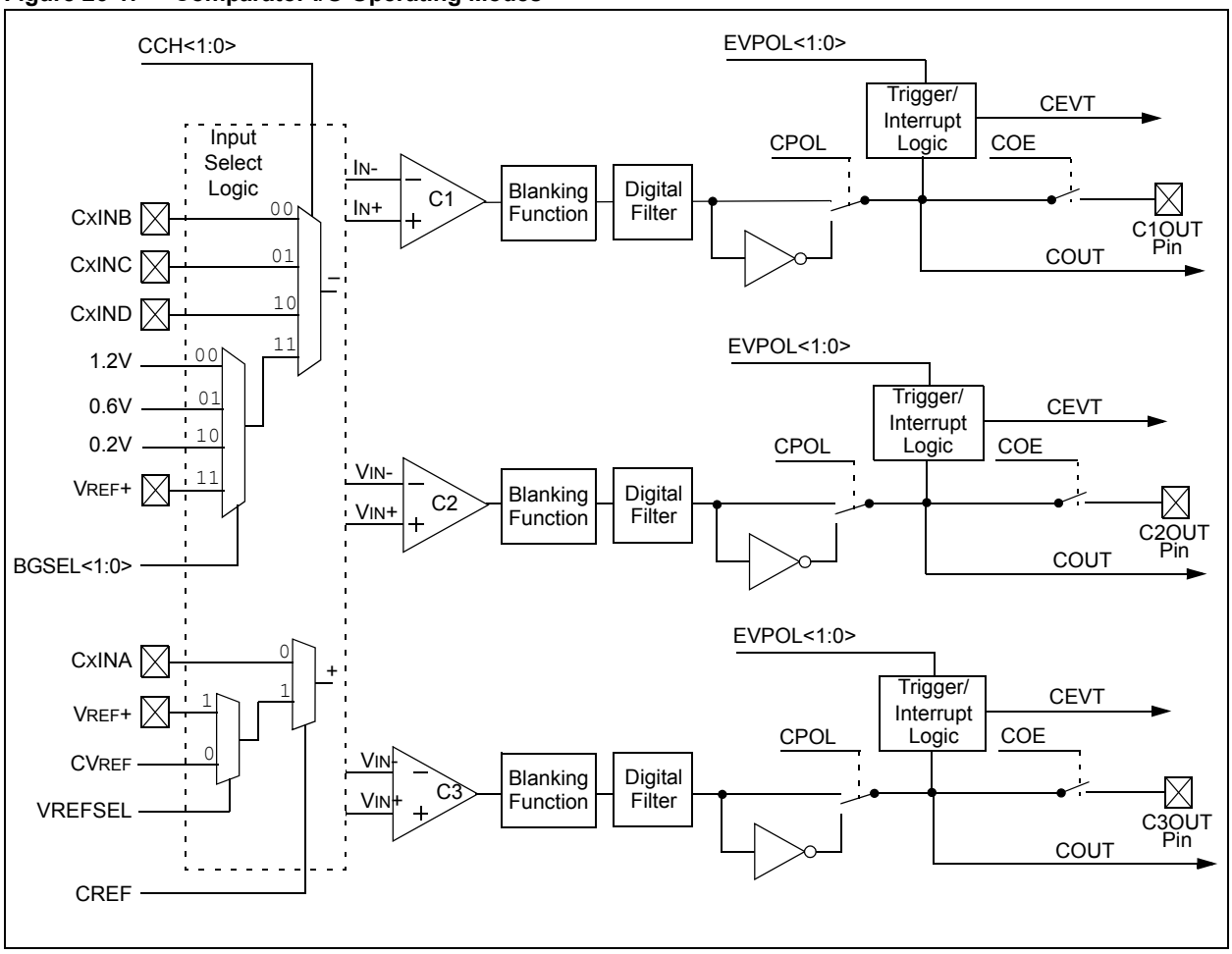
26.1 INTRODUCTION

The dsPIC33E/PIC24E Comparator module provides three comparators that can be configured in different ways. As illustrated in Figure 26-1, individual comparator options are specified by the Comparator module's Special Function Register (SFR) control bits. The following options allow users to:

- Select the edge for trigger and interrupt generation
- Select low-power control
- Configure the comparator voltage reference and band gap
- Configure output blanking and masking

The comparator operating mode is determined by the input selections (that is, whether the input voltage is compared to a second input voltage, to an internal voltage band gap reference, or to an internal reference voltage). The internal reference voltage is generated by a resistor ladder network that is configured by the Comparator Voltage Reference Control register (CVRCON) (see Register 26-6).

Figure 26-1: Comparator I/O Operating Modes



26.2 COMPARATOR REGISTERS

The Comparator module uses the following six registers:

- **CMSTAT: Comparator Status Register**

  This register enables control over the operation of all comparators when the device enters Idle mode. In addition, it provides the status of all comparator results, as well as all of the comparator outputs and event bits, which are replicated as read-only bits in the CMSTAT register.

- **CMxCON: Comparator Control Register** (where x = 1, 2, or 3)

  This register allows the application program to enable, configure, and interact with the individual comparators.

- **CMxMSKSRC: Comparator Mask Source Select Control Register**

  This register allows the application program to select sources for the inputs to the blanking function.

- **CMxMSKCON: Comparator Mask Gating Control Register**

  This register allows the application program to specify the blank function logic.

- **CMxFLTR: Comparator Filter Control Register**

  This register enables comparator filter configuration.

- **CVRCON: Comparator Voltage Reference Control Register**

This register allows the application program to enable, configure and interact with the comparator internal voltage reference generator (for more information, see **26.6 "Comparator Voltage Reference Generator"**).

Register 26-1: CMSTAT: Comparator Status Register

R/W-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	C3OUT	C2OUT	C1OUT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMSIDL:** Stop in Idle Mode bit
1 = Discontinue operation of all comparators when device enters Idle mode
0 = Continue operation of all comparators in Idle mode

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **C3EVT:** Comparator 3 Event Status bit
Reflects the event status of Comparator 3

bit 9 **C2EVT:** Comparator 2 Event Status bit
Reflects the event status of Comparator 2

bit 8 **C1EVT:** Comparator 1 Event Status bit
Reflects the event status of Comparator 1

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator 3 Output Status bit
Reflects the value of the Comparator 3 output

bit 1 **C2OUT:** Comparator 2 Output Status bit
Reflects the value of the Comparator 2 output

bit 0 **C1OUT:** Comparator 1 Output Status bit
Reflects the value of the Comparator 1 output

Register 26-2: CMxCON: Comparator Control Register

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	CLPWR	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12 **CLPWR:** Comparator Low Power Mode Select bit
1 = Comparator operates in low-power mode
0 = Comparator does not operate in low-power mode

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/Event/Interrupt generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/Event/Interrupt generated only on high to low transition of the polarity-selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output
01 = Trigger/Event/Interrupt generated only on low to high transition of the polarity-selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output
00 = Trigger/Event/Interrupt generation is disabled

Register 26-2: CMxCON: Comparator Control Register (Continued)

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (non-inverting input)

1 = Non-inverting input connects to internal selectable reference voltage specified by the VREFSEL bit in the CVRCON register

0 = Non-inverting input connects to CxINA pin

Comparator Reference Selection Encoding

CREF	Source
1	CVREF or VREF+
0	CxINA

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits

11 = Inverting input of comparator connects to internal selectable reference voltage specified by the BGSEL<1:0> bits in the CVRCON register

10 = Inverting input of comparator connects to CxIND pin

01 = Inverting input of comparator connects to CxINC pin

00 = Inverting input of comparator connects to CxINB pin

Comparator Negative Input Selection Encoding

CCH<1:0>	Source
1 1	1.2V, 0.6V, 0.2V OR VREF+
1 0	CxIND
0 1	CxINC
0 0	CxINB

Register 26-3: CMxMSKSRC: Comparator Mask Source Select Control Register

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SELSRCB<3:0>				SELSRCA<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

Register 26-3: CMxMSKSRC: Comparator Mask Source Select Control Register (Continued)

bit 3-0 **SELSRCA<3:0>:** Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

Register 26-4: CMxMSKCON: Comparator Mask Gating Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **HLMS:** High or Low Level Masking Select bits
1 = The comparator deasserted state is '1', and the masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The comparator deasserted state is '0', and the masking (blanking) function will prevent any asserted ('1') comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate C Input Enable bit
1 = C input enabled as input to OR gate
0 = C input disabled as input to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = C input (inverted) enabled as input to OR gate
0 = C input (inverted) disabled as input to OR gate

bit 11 **OBEN:** OR Gate B Input Enable bit
1 = B input enabled as input to OR gate
0 = B input disabled as input to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = B input (inverted) enabled as input to OR gate
0 = B input (inverted) disabled as input to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
1 = A input enabled as input to OR gate
0 = A input disabled as input to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = A input (inverted) enabled as input to OR gate
0 = A input (inverted) disabled as input to OR gate

bit 7 **NAGS:** Negative AND Gate Output Select
1 = Negative (inverted) output of the AND gate is enabled as the input to the OR gate
0 = Negative (inverted) output of the AND gate is disabled as input to the OR gate

bit 6 **PAGS:** Positive AND Gate Output Select
1 = Positive output of the AND gate is enabled as the input to the OR gate
0 = Positive output of the AND gate is disabled as input to the OR gate

bit 5 **ACEN:** AND Gate A1 C Input Enable bit
1 = C input enabled as input to AND gate A1
0 = C input disabled as input to AND gate A1

bit 4 **ACNEN:** AND Gate A1 C Input Enable bit
1 = C input enabled as input to AND gate A1
0 = C input disabled as input to AND gate A1

Register 26-4: CMxMSKCON: Comparator Mask Gating Control Register (Continued)

bit 3 **ABEN:** AND Gate A1 B Input Enable bit
1 = B input enabled as input to AND gate A1
0 = B input disabled as input to AND gate A1

bit 2 **ABNEN:** AND Gate A1 B Input Inverted Enable bit
1 = B input (inverted) enabled as input to AND gate A1
0 = B input (inverted) disabled as input to AND gate A1

bit 1 **AAEN:** AND Gate A1 A Input Enable bit
1 = A input enabled as input to AND gate A1
0 = A input disabled as input to AND gate A1

bit 0 **AANEN:** AND Gate A1 A Input Inverted Enable bit
1 = A input (inverted) enabled as input to AND gate A1
0 = A input (inverted) disabled as input to AND gate A1

Register 26-5: CMxFLTR: Comparator Filter Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	I-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL<2:0>:** Comparator Filter Input Clock Select bits
111 = T5CLK(1)
110 = T4CLK(1)
101 = T3CLK(1)
100 = T2CLK(1)
011 = SYNCO2(2)
010 = SYNCO1(2)
001 = FOSC(3)
000 = FCY(3)

bit 3 **CFLTREN:** Comparator Output Digital Filter Enable bit
1 = Digital filter enabled
0 = Digital filter disabled

bit 2-0 **CFDIV<2:0>:** Comparator Output Filter Clock Divide Select bits
111 = Clock Divide 1:128
110 = Clock Divide 1:64
101 = Clock Divide 1:32
100 = Clock Divide 1:16
011 = Clock Divide 1:8
010 = Clock Divide 1:4
001 = Clock Divide 1:2
000 = Clock Divide 1:1

Note 1: For more information, refer to the specific device data sheet or section (**Section 11. "Timers"** (DS70362) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

2: For more information, refer to the specific device data sheet or **Section 14. "High-Speed PWM"** in the *"dsPIC33E/PIC24E Family Reference Manual"*.

3: For more information, refer to the specific device data sheet or **Section 8. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

Register 26-6: CVRCON: Comparator Voltage Reference Control Register

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	VREFSEL	BGSEL<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE(1)	CVRR	CVRSS	CVR<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = Reference source for non-inverting input is VREF+
0 = Reference source for non-inverting input is 4-bit DAC reference

bit 9-8 **BGSEL<1:0>:** Band Gap Reference Source Select bits
11 = Reference source for inverting input is VREF+
10 = Reference source for inverting input is 0.2 V (nominal)
01 = Reference source for inverting input is 0.6 V (nominal)
00 = Reference source for inverting input is 1.2 V (nominal)

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit powered on
0 = Comparator voltage reference circuit powered down

bit 6 **CVROE:** Comparator Voltage Reference Output Enable bit(1)
1 = Voltage level is output on CVREF pin
0 = Voltage level is disconnected from CVREF pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size
0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection 0 ≤ CVR3:CVR0 ≤ 15 bits
When CVRR = 1:
CVREFIN = (CVR<3:0>/24) • (CVRSRC)
When CVRR = 0:
CVREFIN = 1/4 • (CVRSRC) + (CVR<3:0>/32) • (CVRSRC)

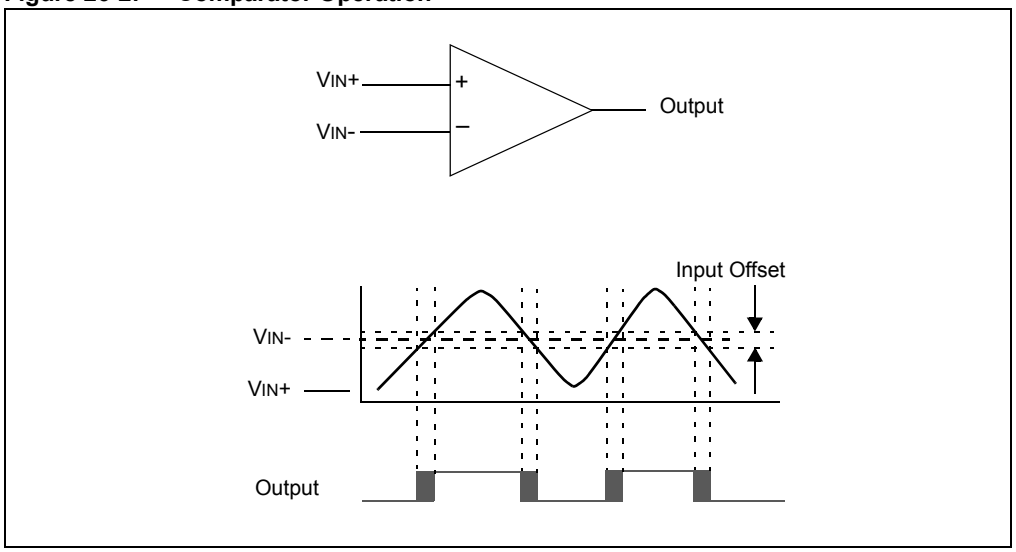
Note 1: CVROE overrides the TRIS bit setting.

26.3 COMPARATOR OPERATION

The operation of a typical comparator is illustrated in Figure 26-2, along with the relationship between the analog input levels and the digital output. Depending on the comparator operating mode, the monitored analog signal is compared to either an external or internal voltage reference. Each of the comparators can be configured to use the same or different reference sources. For example, one comparator can use an external reference while the others use the internal reference. For more information on comparator operation, see **26.6 "Comparator Voltage Reference Generator"**.

In Figure 26-2, the external reference, VIN-, is a fixed external voltage. The analog signal present at VIN+ is compared to the reference signal at VIN-, and the digital output of the comparator is created when the difference is great enough. When VIN+ is less than VIN-, the output of the comparator is a digital low level. When VIN+ is greater than VIN-, the output of the comparator is a digital high level. The shaded areas of the output represent the area of uncertainty due to input offsets and response time. The polarity of the comparator output can be inverted, so that it is a digital low level when VIN+ is greater than VIN-.

Figure 26-2: Comparator Operation



Input offset represents the range of voltage levels within which the comparator trip point can occur. The output can switch at any point in this offset range. Response time is the minimum time required for the comparator to recognize a change in input levels.

26.4 COMPARATOR CONFIGURATION

Each of the three comparators in the Comparator module is configured independently by various control bits in the following registers:

- Comparator Status (CMSTAT) register (Register 26-1)
- Comparator Control (CMxCON) register (Register 26-2)
- Comparator Mask Source Control (CMxMSKSRC) register (Register 26-3)
- Comparator Mask Gating Control (CMxMSKCON) register (Register 26-4)
- Comparator Filter Control (CMxFLTR) register (Register 26-5)
- Comparator Voltage Reference Control (CVRCON) register (Register 26-6)

26.4.1 Comparator Enable/Disable

The comparator under control may be enabled or disabled using the corresponding CON bit of the CMxCON register. When the comparator is disabled, the corresponding trigger and interrupt generation is disabled when CON = 0.

It is recommended to first configure the CMxCON register with all bits to the desired value, and then set the CMxCON<CON> bit.

26.4.2 Comparator Output Blanking Function

In many power control and motor control applications, there are periods of time in which the inputs to the analog comparator are known to be invalid. The blanking (masking) function enables the user to ignore the comparator output during predefined periods of time. In this document, the terms ‘masking’ and ‘blanking’ are used interchangeably.

Figure 26-3 illustrates a block diagram of the comparator blanking circuitry. A blanking circuit is associated with each analog comparator.

Each comparator’s blanking function has three user selectable inputs:

- MAI (Mask A Input)
- MBI (Mask B Input)
- MCI (Mask C Input)

The MAI, MBI and MCI signal sources are selected through the SELSRCA<3:0>, SELSRCB<3:0> and SELSRCC<3:0> bit fields in the CMxMSKSRC registers.

The MAI, MBI and the MCI signals are fed into an AND-OR function block, which enables the user to construct a blanking (masking) signal from these inputs.

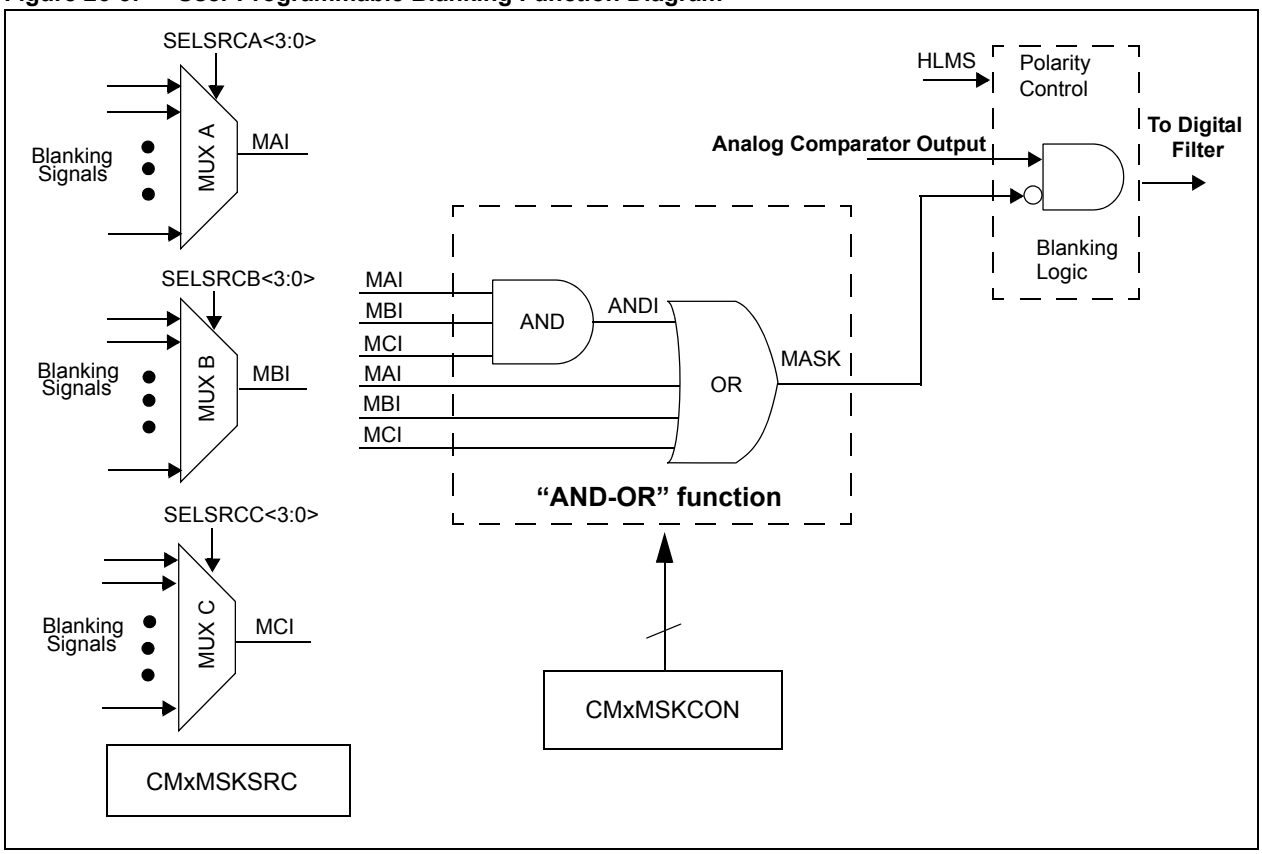
The blanking (masking) function is disabled following a system Reset.

The HLMS bits in the CMxMSKCON registers configure the masking logic to operate properly depending on the default (deasserted) state of the comparators.

If the comparator is configured for ‘positive logic’ so that a ‘0’ represents a deasserted state and the comparator output is a ‘1’ when it is asserted, the HLMS bit should bet set to ‘0’ so that the blanking function (assuming the blanking function is active) will prevent the ‘1’ signal of the comparator from propagating through the module.

If the comparator is configured for ‘negative logic’ so that a ‘1’ represents a deasserted state and the comparator output is a ‘0’ when it is asserted, the HLMS bit should be set to a ‘1’ so that the blanking function (assuming blanking function is active) will prevent the ‘0’ signal of the comparator from propagating through the module.

Figure 26-3: User Programmable Blanking Function Diagram



26.4.3 Digital Output Filter

In many motor and power control applications, the analog comparator input signals can be corrupted by the large electromagnetic fields generated by the associated external switching power transistors. Corruption of the analog input signals to the comparator can cause unwanted comparator output transitions. The programmable digital output filter can minimize the effects of input signal corruption.

The digital filter requires three consecutive input samples to be similar before the output of the filter can change state. Assuming the current state is 'zero', a string of inputs such as '001010110111' will only yield an output state of 'one' at the end of the example sequence after the three consecutive '1's. Similarly, a sequence of three consecutive '0's are required before the output will change to a zero state.

Because of the requirement of three similar consecutive states for the filter, the chosen digital filter clock period must be one-third or less than the maximum desired comparator response time.

The digital filter is enabled by setting the CFLTREN bit in the CMxFLTR control register. The CFDIV<2:0> bits in the CMxFLTR register select the clock divider ratio for the clock signal input to the digital filter block. The CFSEL<2:0> bits in the CMxFLTR register select the desired clock source for digital filter. The digital filter is disabled (bypassed) following a system Reset.

26.4.4 Comparator Polarity Selection

To provide maximum flexibility, the output of the comparator may be inverted using the CPOL bit in the CMxCON register. This is functionally identical to reversing the inverting and non-inverting inputs of the comparator for a particular mode.

The CPOL bit should be changed only when the comparator is disabled (CON = 0). Internal logic will prevent the generation of any corresponding triggers or interrupts when CON = 0. The logic allows both the CON and CPOL bits to be set with a single register write.

26.4.5 Event Polarity Selection

In addition to a programmable comparator output polarity, this module also allows software selection for trigger/interrupt edge polarity, through the EVPOL<1:0> bits in the corresponding CMxCON register. This feature allows independent control of the comparator output, as seen on any external pins, and the trigger/interrupt generation.

Note:	The corresponding comparator must be enabled (CON = 1) for the specific trigger/interrupt generation to be enabled.

26.4.6 Comparator Reference Input Selection

The input to the non-inverting input of the comparator, also known as the reference input, can be selected between the following three settings:

- CxINA pin (CON = 1, CREF = 0)
- Internal CV_{REF} voltage (CON = 1, CREF = 1)
- None (CON = 0, CREF = x). In this case, the comparator output status will be indeterminate, and associated trigger/interrupt generation is disabled

26.4.7 Comparator Channel Selection

The input to the inverting input of the comparator, also known as the channel input, can be selected between the following five settings:

- CxINB pin (CON = 1, CCH<1:0> = 2'b00)
- CxINC pin (CON = 1, CCH<1:0> = 2'b01)
- CxIND pin (CON = 1, CCH<1:0> = 2'b10)
- Band Gap Reference (CON = 1, CCH<1:0> = 2'b11). The source of the band gap reference can be selected by the user-assigned application through the BGSEL<1:0> bits in the Comparator Voltage Reference Control register (CVRCON<9:8>).
- None (CON = 0, CCH<1:0> = 2'bxx). In this case, the comparator output status will be indeterminate, and associated trigger/interrupt generation is disabled.

26.4.8 Low-Power Selection

Depending on the capabilities of the comparator modules, this interface provides a Low-power mode selection bit (CLPWR). Using this bit, a user can trade off power consumption for the speed of the comparator.

When CLPWR = 0, standard power mode is active. When CLPWR = 1, the low-power setting of the corresponding comparator is enabled.

Note:	The comparator power setting should not be changed while CON = 1.

26.4.9 Comparator Event Status Bit

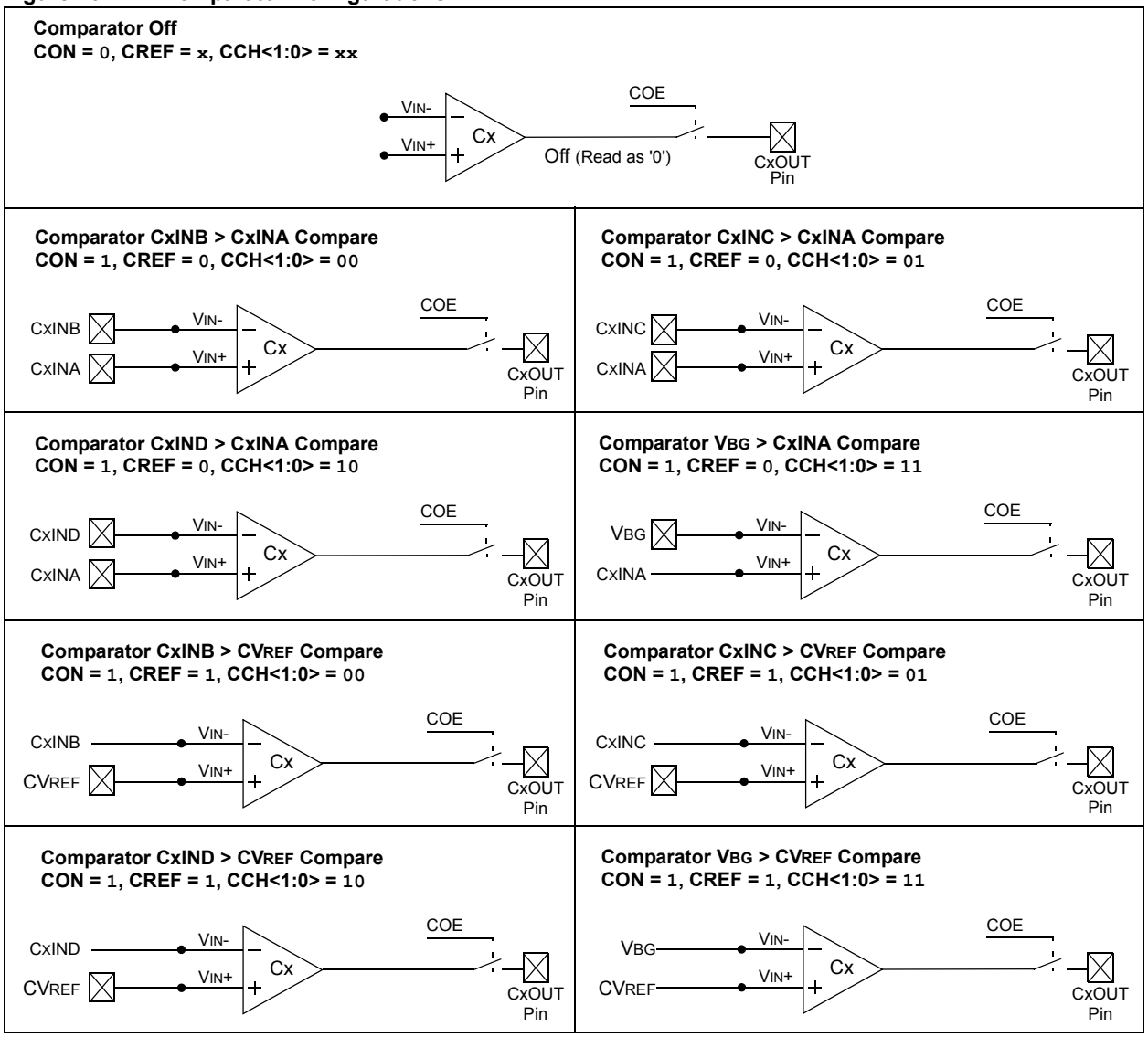
The Comparator Event Status (CEVT) bit (CMxCON<9>) reflects whether or not the comparator has gone through the preconfigured event. After the bit is set, all future triggers and interrupts from the corresponding comparator will be blocked until the user-assigned application clears the CEVT bit. Clearing the CEVT bit begins re-arming the trigger. Once the CEVT bit is cleared, it takes an extra CPU cycle for the comparator triggers to be fully re-armed.

26.4.10 Status Register

To provide an overview of all comparator results, all the comparator outputs (CMxCON<COUT>) and event bits (CMxCON<CEVT>) are replicated as status bits in the CMSTAT register.

These bits are read-only and can be altered only by manipulating the corresponding CMxCON register or the comparator input signals.

Figure 26-4: Comparator Configurations



26.5 COMPARATOR INTERRUPTS

The Comparator Interrupt Flag (CMIF) bit (IFS1<2>) is set when the synchronized output value of any of the three comparator changes with respect to the last read value. These status bits reflect the following output change:

- **C1EVT** – Comparator 1 Event (CMSTAT<8>)
- **C2EVT** – Comparator 2 Event (CMSTAT<9>)
- **C3EVT** – Comparator 3 Event (CMSTAT<10>)

User-assigned software can read the CxEVT and CxOUT bits to determine the change that occurred. Because it is possible to write a '1' to this register, a simulated interrupt can be software initiated. Both the CMIF and CxEVT bits must be reset by clearing them in software. These bits can be cleared in the Interrupt Service Routine. For more information, refer to the **Section 6. "Interrupts"** (DS70600) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

Note:	The comparison required for generating interrupts is based on the current comparator state and the last read value of the comparator outputs. Reading the C1OUT, C2OUT and C3OUT bits in the CMxCON register will update the values used for the interrupt generation.

26.5.1 Interrupt Operation During Sleep Mode

If a comparator is enabled and the dsPIC33E/PIC24E device is placed in Sleep mode, the comparator remains active. If the Comparator interrupt is enabled in the Interrupt module, it remains functional. Under these conditions, a comparator interrupt event will wake-up the device from Sleep mode.

Each operational comparator consumes additional current. To minimize power consumption in Sleep mode, turn off the comparators before entering Sleep mode by disabling the CON bits (CMxCON<11:10>). If the device wakes up from Sleep mode, the contents of the CMxCON register are not affected. For more information on Sleep mode, refer to the **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70615) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

26.5.2 Interrupt Operation During Idle Mode

The comparator remains active in Idle mode. Comparator interrupt operation during idle mode is controlled by the Comparator Idle Mode (CMIDL) bit (CMSTAT<15>). If CMIDL = 0, normal interrupt operation continues. If CMIDL = 1, the comparator continues to operate, but it does not generate interrupts.

For more information on Idle mode, refer to the **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70615) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

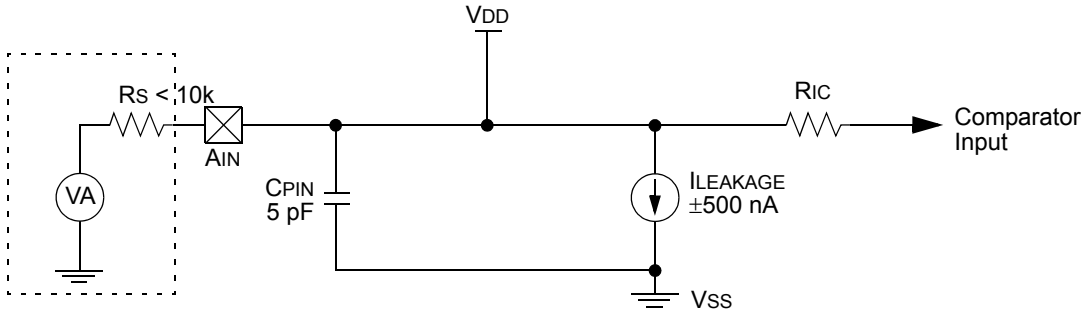
26.5.3 Effects of a Reset State

A device Reset forces the CMxCON register to its Reset state, causing the comparator modules to be turned off (CON = 0). However, the input pins multiplexed with analog input sources are configured as analog inputs by default on device Reset. The I/O configuration for these pins is determined by the setting of the ADxPCFGL or ADxPCFGH register. Therefore, device current is minimized when analog inputs are present at Reset time.

26.5.4 Analog Input Connection Considerations

A simplified circuit for an analog input is illustrated in Figure 26-5. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have little leakage current.

Figure 26-5: Comparator Analog Input Model



Legend:

CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC= Interconnect Resistance
RS = Source Impedance

26.6 COMPARATOR VOLTAGE REFERENCE GENERATOR

The internal comparator voltage reference is derived from a 16-tap resistor ladder network that provides a selectable voltage level, as illustrated in Figure 26-6. This resistor network generates the internal voltage reference for the analog comparators.

This voltage generator network is managed by the Comparator Voltage Reference Control (CVRCON) register (see Register 26-6) through these control bits:

- **CVREN** – Comparator Voltage Reference Enable (CVRCON<7>)

  This control bit enables the voltage reference circuit.

- **CVROE** – Comparator Voltage Reference Output Enable (CVRCON<6>)

  This control bit enables the reference voltage to be placed on the CVREF pin. When enabled, this bit overrides the corresponding TRIS bit setting.

- **VREFSEL** – Voltage Reference Select bit (CVRCON<10>)

  This control bit specifies whether the reference source is external (VREF+), or it is obtained from the 4-bit DAC output.

- **CVRSS** – Comparator Voltage Reference Source Selection (CVRCON<4>)

  This control bit specifies that the source (CVRSS) for the voltage reference circuit is either the device voltage supply (AVDD and AVSS) or an external reference (VREF+ and VREF–).

- **CVRR** – Comparator Voltage Reference Range Selection (CVRCON<5>)

  This control bit selects one of the two voltage ranges covered by the 16-tap resistor ladder network:

  - 0 to 0.67 CVRSRC
  - 0.25 CVRSRC to 0.75 CVRSRC

  The range selected also determines the voltage increments available from the resistor ladder taps (see **26.6.1 "Configuring the Comparator Voltage Reference"**).

- **CVR<3:0>** – Comparator Voltage Reference Value Selection (CVRCOM<3:0>)

  These bits designate the resistor ladder tap position.

Table 26-1 lists the voltage at each tap for both ranges with CVRSRC = 3.3V.

Figure 26-6: Comparator Voltage Reference Block Diagram

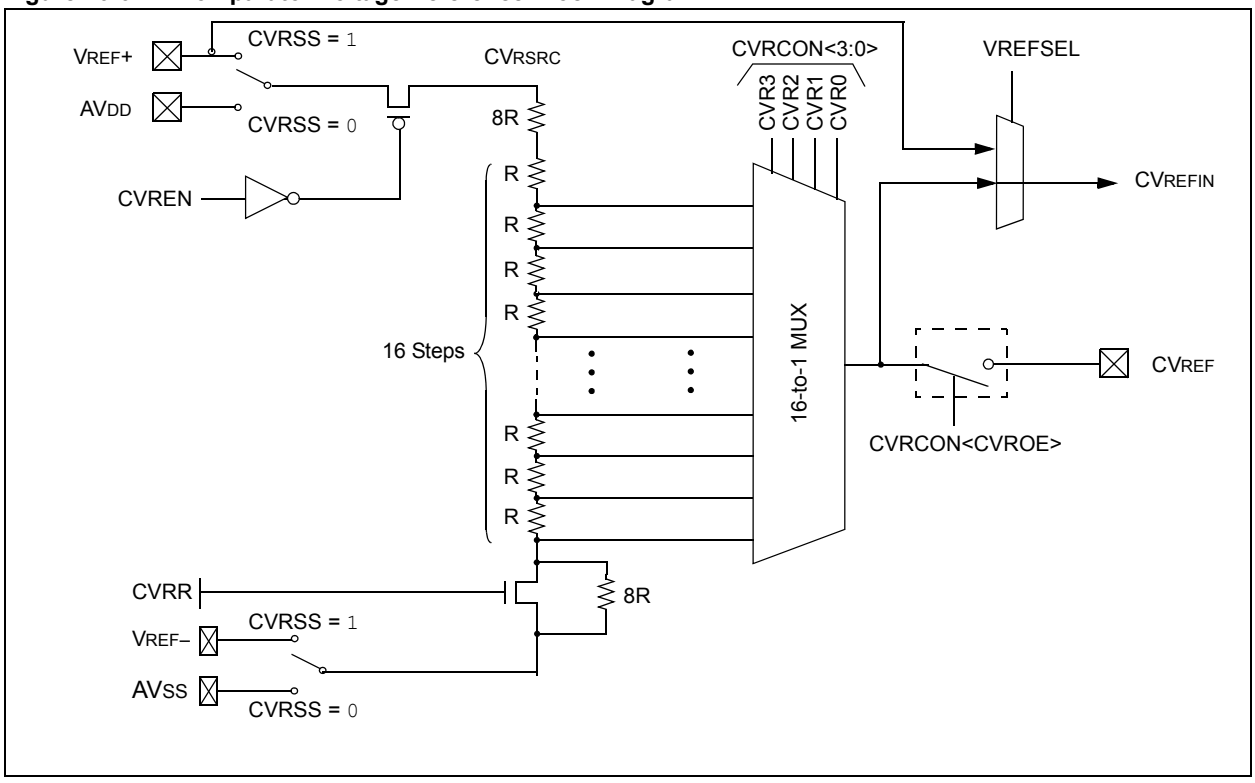


Table 26-1: Typical Voltage Reference with CVRSRC = 3.3V

CVR<3:0>	Tap	Voltage Reference	
		CVRR = 0	CVRR = 1
0000	0	0.83V	0.00V
0001	1	0.93V	0.14V
0010	2	1.03V	0.28V
0011	3	1.13V	0.41V
0100	4	1.24V	0.55V
0101	5	1.34V	0.69V
0110	6	1.44V	0.83V
0111	7	1.55V	0.96V
1000	8	1.65V	1.10V
1001	9	1.75V	1.24V
1010	10	1.86V	1.38V
1011	11	1.96V	1.51V
1100	12	2.06V	1.65V
1101	13	2.17V	1.79V
1110	14	2.27V	1.93V
1111	15	2.37V	2.06V

26.6.1 Configuring the Comparator Voltage Reference

The voltage range selected by the CVRR bit determines the size of the steps selected by the CVR<3:0> bits. One range (CVRR = 0) provides finer resolution by offering smaller voltage increments for each step. The equations used to calculate the comparator voltage reference are as follows:

If CVRR = 1:
Voltage Reference = ((CVR<3:0>)/24) • (CVRSRC)

If CVRR = 0:
Voltage Reference = (CVRSRC/4) + ((CVR<3:0>)/32) • (CVRSRC)

26.6.2 Voltage Reference Accuracy/Error

The full voltage reference range cannot be realized because the transistors on the top and bottom of the resistor ladder network (Figure 26-6) keep the voltage reference from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the voltage reference output changes with fluctuations in the reference source. For reference voltage accuracy, refer to the “Electrical Characteristics” section of the data sheet for the device you are using.

26.6.3 Operation During Sleep Mode

When the device wakes up from Sleep mode through an interrupt or a Watchdog Timer time-out, the contents of the CVRCON register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

26.6.4 Effects of a Reset

A device Reset has the following effects:

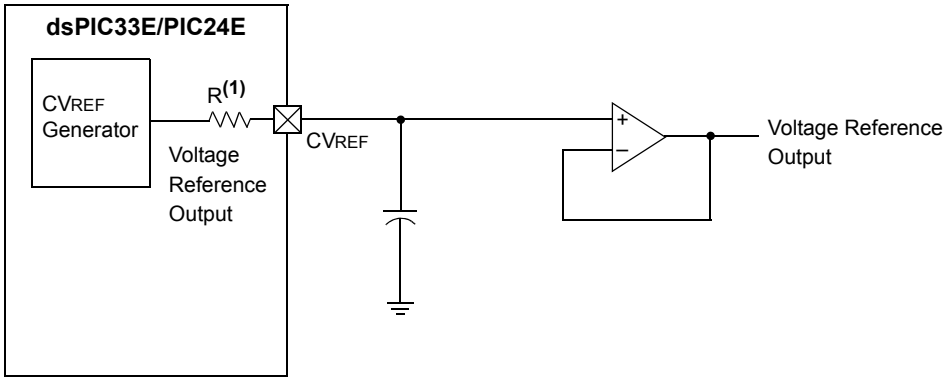
- Disables the voltage reference by clearing the CVREN bit (CVRCON<7>)
- Disconnects the reference from the CVREF pin by clearing the CVROE bit (CVRCON<6>)
- Selects the high-voltage range by clearing the CVRR bit (CVRCON<5>)
- Clears the CVR value bits (CVRCON<3:0>)

26.6.5 Connection Considerations

The voltage reference generator operates independently of the Comparator module. The output of the reference generator is connected to the CVREF pin if the CVROE bit (CVRCON<6>) is set. Enabling the voltage reference output onto the I/O when it is configured as a digital input will increase current consumption. Configuring the port associated with CVREF as a digital output, with CVRSS enabled, will also increase current consumption.

The CVREF output pin can be used as a simple Digital-to-Analog output with limited drive capability. Due to this limited current drive capability, a buffer must be used on the voltage reference output for external connections to CVREF. Figure 26-7 illustrates a buffering technique example.

Figure 26-7: Comparator Voltage Reference Output Buffer Example



Note 1: R is dependent upon the comparator voltage reference control CVRR bits (CVRCON<5>) and CVR<3:0> value bits (CVRCON<3:0>).

26.7 REGISTER MAP

A summary of the registers associated with the Comparator module is provided in Table 26-2.

Table 26-2: Comparator Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000
CMxCON	CON	COE	CPOL	CLPWR	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CMxMSKSRC	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CMxMSKCON	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CMxFLTR	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CVRCON	—	—	—	—	—	VREFSEL	BGSEL<1:0>		CVREN	CVROE	CVRR	CVRSS	CVR<3:0>				0000

26.8 DESIGN TIPS

Question 1: ***Why is my voltage reference not what I expect?***

Answer: Any variation of the voltage reference source will translate directly onto the CVREF pin. Also, ensure that you have correctly calculated (specified) the voltage divider which generates the voltage reference.

Question 2: ***Why is my voltage reference not at the expected level when I connect CVREF into a low-impedance circuit?***

Answer: The voltage reference module is not intended to drive large loads. A buffer must be used between the CVREF pin and the load of the dsPIC33E/PIC24E device (see Figure 26-7).

26.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33E/PIC24E device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Comparator module are:

Title	Application Note #
Make a Delta-Sigma Converter Using a Microcontroller's Analog Comparator Module	AN700
A Comparator Based Slope ADC	AN863

Note: Visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33E/PIC24E family of devices.

26.10 REVISION HISTORY

Revision A (November 2008)

This is the initial release of this document.

Revision B (April 2010)

This version of the document includes the following updates:

- Replaced Figure 26-1: Comparator I/O Operating Modes
- Updated the CMxCON: Comparator Control Register (Register 26-2):
  - Changed the default POR values for the COE COUT and EVPOL<1:0> bits
  - Updated the selection encoding tables for the CREF and CCH<1:0> bits
  - Updated the CREF = 1 definition
  - Updated the CCH<1:0> = 11 definition
- Updated the CMxMSKSRC: Comparator Mask Source Select Control Register (Register 26-3):
  - Renamed the SELSRC_A, SELSRC_B, and SELSRC_C bits to SELSRCA, SELSRCB, and SELSRCC
  - Changed the bit value definitions for SELSRCA, SELSCRB, and SELSRCC
- Updated the CMxMSKCON: Comparator Mask Gating Control Register (Register 26-4):
  - Removed the word inverted from the OCEN, OBEN, ACEN, and ABEN bit definitions
- Added Note 1, Note 2, and Note 3 and updated the CFSEL<2:0> bit definition in the CMxFLTR: Comparator Filter Control Register (Register 26-5)
- Updated the bit value definitions for the VREFSEL and BGSEL<1:0> bits in the CVRCON: Comparator Voltage Reference Control Register (Register 26-6)

NOTES:

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