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TC4426/27/28 System Design Practice

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INTRODUCTION

The TC4426/4427/4428 are high-speed power MOSFET drivers built using Microchip Technology's tough CMOS process. They are improved versions of the earlier TC426/427/428 family of high-speed power MOSFET drivers (with which they are pin compatible) and are capable of giving reliable service in far more demanding electrical environments. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4kV of electrostatic discharge.

As a result, the TC4426/4427/4428 are much easier to use, more flexible in operation, and much more forgiving than any other drivers (CMOS or bipolar) currently available. Because they are fabricated in CMOS, they dissipate a minimum of power and provide rail-to-rail voltage swings to ensure the logic state of any load they are driving.

The TC4426/27/28 fast switching times are made possible by a low impedance CMOS output stage. The high peak currents make 30nsec rise/fall times possible.

The rapid rise/fall times do, however, require systems be designed with adequate power supply decoupling and stray lead inductance minimization. Practices which are adequate for 1µsec rise/fall times and 20mA peak currents will not be adequate with the TC4426 family. The same laws of physics apply in both systems. The results may be negligible in one and of prime importance in another.

For example, a 0.1µH power lead inductance (4" of 0.025" diameter wire) can cause a voltage spike 1000 times larger in a fast system with an unbypassed supply.

Low Speed System	**High Speed System**
L_S = 0.1µH	L_S = 0.1µH
ΔV_{OUT} = 18V	ΔV_{OUT} = 18V
t = 1µsec	t = 30nsec
I_{PK} = 20mA	I_{PK} = 600mA
C_L = 1000pF	C_L = 1000pF
ΔV_{SUPPLY} = L di/dt	ΔV_{SUPPLY} = L di/dt
= 2mV	= 2.0V

The system design practices needed are not difficult to apply. The simple good engineering practice of bypassing the power supply, minimizing stray lead inductance, and grounding unused driver inputs will solve most system problems. Nothing new required — just a little careful application of techniques common to any high speed CMOS system.

The TC4426 family outputs are CMOS. Low quiescent power and high output voltage drive (very important with 5V supply operation) result. Since the outputs are CMOS the potential for activating a parasitic SCR exists. This must be avoided to prevent potential device destruction. If the TC4426 output, like any CMOS chip, is driven below ground or above the positive power supply an internal parasitic SCR can be turned on. The high current flow can damage the device. The actual TC4426 output stage is shown in Figure 1. The IC layout and simplified equivalent SCR circuit are shown in Figures 2 and 3.

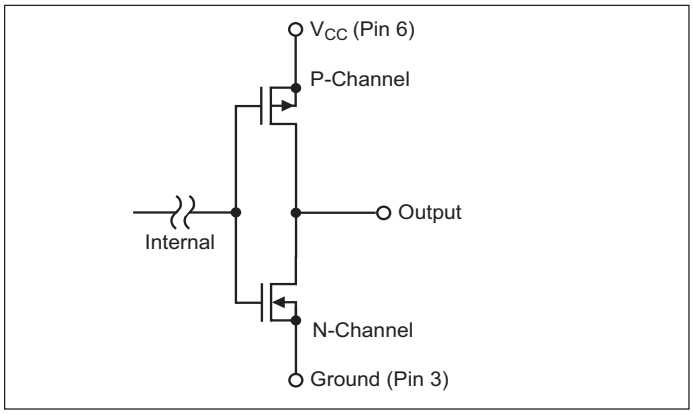


FIGURE 1: TC4426 output.

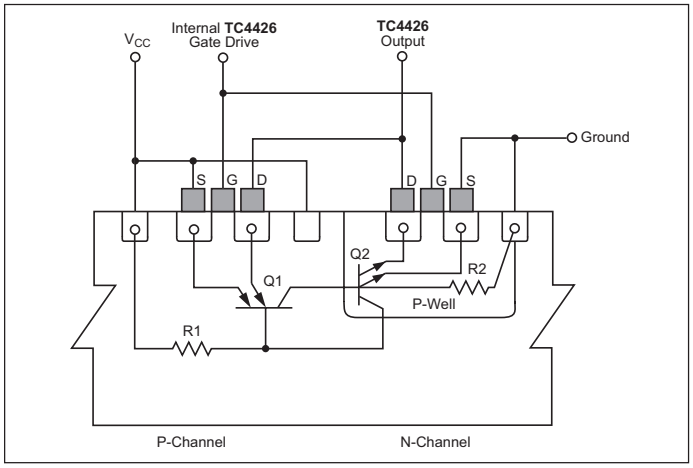


FIGURE 2: Output stage IC layout.

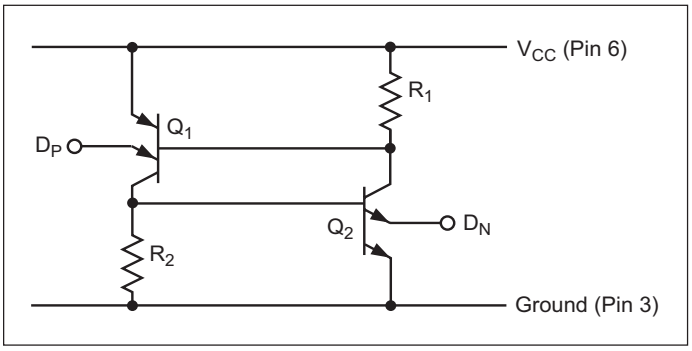


FIGURE 3: Equivalent SCR circuit.

The IC parasitic SCR can be turned on if D_P is raised above V_{CC} or if D_N is forced below ground. An inductive load at the output can also create a voltage swing at the output that exceeds the positive supply or undershoots ground.

If the output is raised above the positive supply, current is injected into the emitter of Q_1 and swept into the collector. The Q_1 collector feeds the base of Q_2 and R_2. When the base of Q_2 reaches 0.6V Q_2 turns on. This forces Q_1 on. The SCR is now "fired" shorting the positive power supply to ground. A similar situation exists when the output is driven below ground.

The internal SCR can also be triggered by excessive voltage on the power supply that results in internal voltage breakdown. The current injected can trigger the SCR action.

By limiting the current injected into the TC4426 output when the output is above the positive power supply latch up is avoided. The limiting current is:

$$I \leq \frac{V_{BE}}{R_2 \text{ II } R_{ONP}}$$

where:

R_{ONP} = ON resistance of P channel device (12Ω max)
V_{BE} = Q_2 base emitter turn on voltage (Approx. 0.6V)
R_2 = Bulk resistance

Assuming the ON resistance dominates, the current should be limited to 40mA. A similar analysis with the output below ground indicates the current pulled out of the TC4426 output should be limited to 60mA. The maximum allowable latch current is temperature sensitive. At high chip temperature the base emitter voltages are reduced. A 1°C rise lowers V_{BE} by 2.2mV.

Current limiting with a series output resistor may not be practical in all systems. The output rise and fall times may increase. An alternate solution uses low forward voltage output clamp diodes to bypass the SCR trigger current around the device.

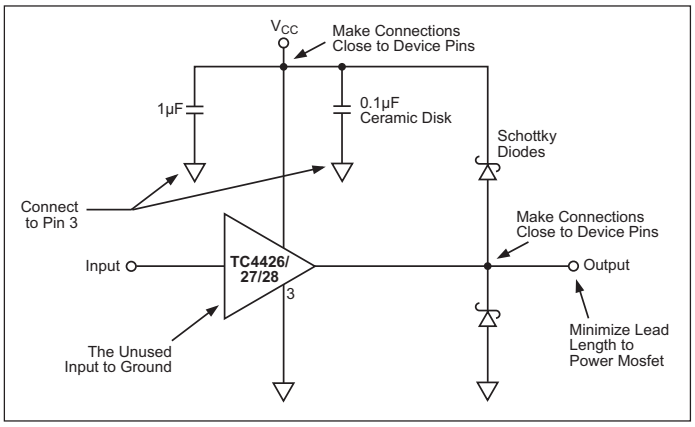


FIGURE 4: Equivalent SCR circuit.

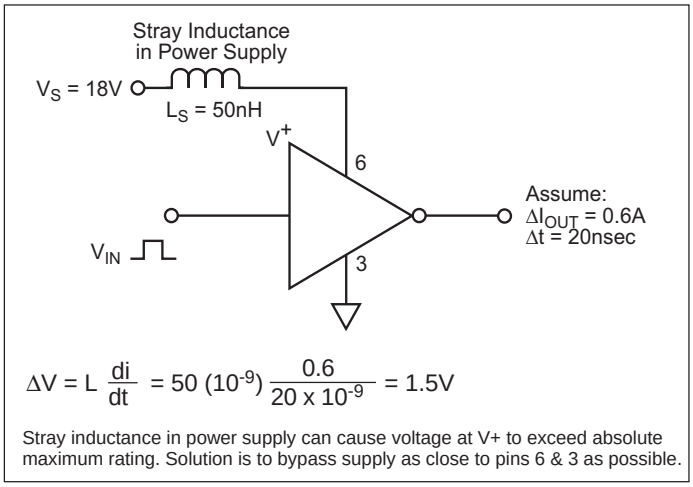


FIGURE 5: Stray supply lead inductance can decrease reliability.

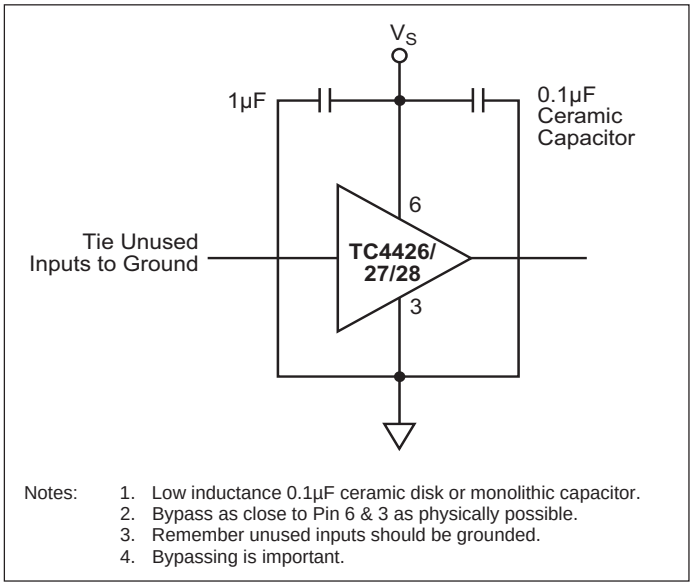


FIGURE 6: Suggested bypass procedure.

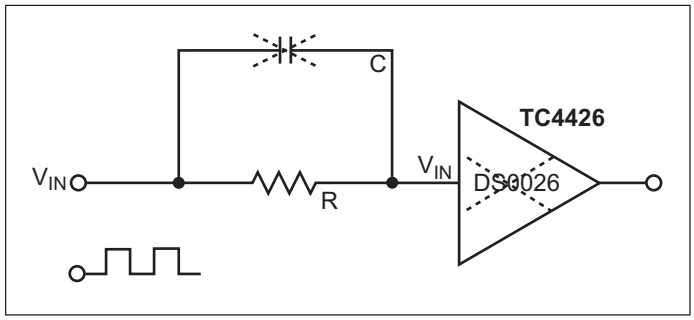


FIGURE 7: TC4426 has CMOS inputs. Speed up capacitors are not required.

External output clamp diodes prevent the TC4426 output from being pulled far enough outside the power supply range to turn on the parasitic SCR. (See App. Note 763).

The external diodes must have a lower forward on base to emitter voltage than the parasitic transistor junctions. Schottky small signal diodes are suitable. Several possible types are:

- Panasonic: P/N MAZH735
- ON Semiconductor: P/N BAS40-04LTI (dual series)
- Zetex: P/N ZHCS1000

To be effective the output clamp diodes must be connected close to the output, supply and ground device pins.

Supply bypass capacitors must also be connected between V_{CC} (Pin 6) and Ground (Pin 3). Connections must be close to the actual device pins (approx. 0.5"). A 0.1µF ceramic disk capacitor in parallel with a 1µF low ESR film capacitor is suggested. Without supply bypassing, power supply lead inductance can cause voltage breakdown. The bypass capacitors also supply the transient current needed during capacitive load charging.

A 10Ω to 15Ω resistor in series with the power supply filters voltage spikes present at the TC4426/27/28 supply terminal. Should latch up occur, this will also limit current. Rise and fall times will not be affected if the recommended supply bypassing is used. See Figure 8.

The DS0026 has a bipolar input. A speed up capacitor is normally used to decrease switching time. Base storage time is reduced. The capacitor causes a voltage spike drive at the input that extends beyond V_{CC} or ground. The TC4426 input is CMOS and does not require a speed up capacitor. In converting DS0026 sockets to the TC4426/27/28 the capacitor should be remove. This will maximize drive to the device and minimize transition time. Benefits include fewer components and reduced insertion costs. See Figure 8.

The TC4426/27/28 outputs feature a low impedance P-channel pull-up MOS device and low impedance N-channel pull-down MOS device. The low resistance outputs are responsible for the 30nsec rise and fall times. The CMOS construction minimizes current drain.

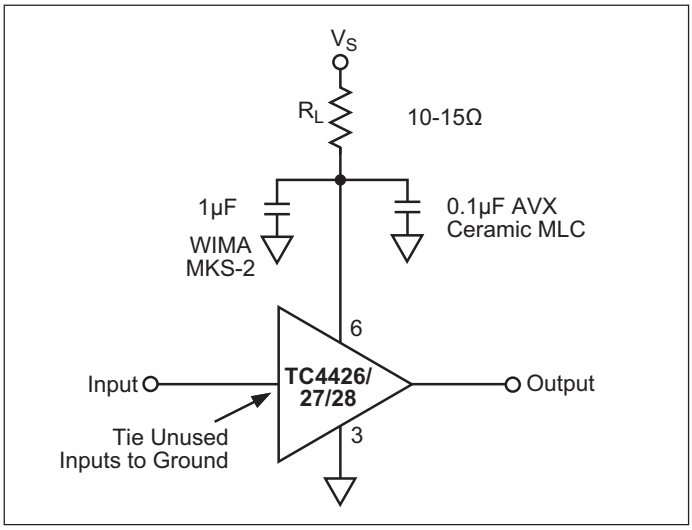


FIGURE 8: R_L current limiting protects device and will not degrade switching speed.

The output N and P channel devices should not be forced to conduct current simultaneously. This can happen if an unused input is left floating. Unused inputs must be connected to ground or the positive supply. A ground connection will minimize steady state supply current. This is common engineering practice followed in CMOS logic system design but is sometimes overlooked during a "quick" bench evaluation. Floating inputs cause excessive current flow and may potentially destroy the driver.

The input drive signal should also have rise and fall times less than 1µsec. This minimizes time spent in the output stage transition region.

Package Power Dissipation

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance the maximum ambient operation temperature is easily calculated. The CerDIP 8-pin package junction to ambient thermal resistance is 150°C/W. At 25°C the package is rated at 800mW maximum dissipation. Maximum allowable chip temperature is 150°C.

Three components make up total package power dissipation:

1. Capacitive load dissipation (P_C)
2. Quiescent power (P_Q)
3. Transition power (P_T)

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation per driver is:

Eq. 1: $P_C = f\ C\ V_S^2$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only 0.6mA total current drain. Logic high signals raise the current to 8mA maximum. The quiescent power dissipation is:

Eq. 2: $P_Q = (V_S)(D)(I_H) + (V_S)(1 – D)(I_L)$

where: I_H = Quiescent current with both inputs high (8mA Max)
I_L = Quiescent current with both inputs low (0.6mA Max)
D = Duty cycle

Transition power dissipation is normally not significant. It arises because the output stage N and P channel MOS transistors are on simultaneously for a very short period when the output changes. The transition package power dissipation power driver is approximately:

Eq. 3: $P_T = f\ V_S\ (1.63nA \times s)$

An example shows the relative magnitude for each term. Both drivers are driven with a 50% duty cycle signal at the same frequency. Capacitive load is the same for each driver.

Example 1:

C = 1000pF
V_S = 18V
D = 50%
f = 200kHz
P_D = Package power dissipation = $P_C + P_Q + P_T$
= 130mW + 77mW + 11.7mW
= 219mW
Max. operating temperature = $T_J – \theta_{JA}\ (P_D)$
= 117°C

where:

T_J = Max. allowable junction temperature (150°C)
θ_{JA} = Junction to ambient thermal resistance (150°C/W, CerDIP)

Table 1 gives the total package power dissipation for several different cases using the formulas previously developed. If only one driver is active divide the package power dissipation numbers by two in Table 1.

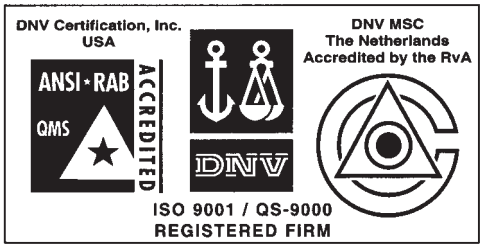
Capacitive Load (pF)	Input Frequency (kHz)	Supply Voltage (V)	Package Power Dissipation CerDIP Package (θ_{JA} = 150°C/W)				
			P_Q (mW)	P_C (mW)	P_T (mW)	P_D (mW)	Max Ambient Operating Temp (°C)
1000	50	18	77	32	3	112	125
1000	100	18	77	65	6	148	125
1000	200	18	77	130	12	219	117
1000	400	18	77	259	23	359	96
1000	1000	18	77	648	59	784	32
1000	50	12	52	14	2	68	125
1000	100	12	52	29	4	85	125
1000	200	12	52	58	8	118	125
1000	400	12	52	115	16	183	123
1000	1000	12	52	288	39	379	93
2000	50	18	77	65	3	145	125
1000	1800	12	52	518	70	640	54
50	4000	18	77	130	235	442	84
1000	100	18	77	65	6	148	125
500	100	18	77	32	6	115	125
500	200	15	65	45	10	120	125
500	100	15	65	23	5	93	125

Notes: 1. Duty Cycle = 50%
2. Each input driven
3. Each output with capacitive load
4. Ambient operating temperature should not exceed 85°C for "EOA" and "EPA" devices or 125°C for "MJA" devices.

TABLE 1: TC4426 package power dissipation.

NOTES:

NOTES:



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