# AD9430 Evaluation Board Modifications for XTAL Oscillator Clocking
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## INTRODUCTION

The AD9430-170/210-CMOS evaluation board is designed to accommodate clocking from an external signal source or an on-board XTAL oscillator. The board, as shipped, interfaces with a single-ended 1 V p-p sine wave source applied to SMA J5 on the board. This signal is converted to differential LVPECL levels by an on-board differential receiver, an LVEL16.

The board can be modified as follows:

The differential receiver must be removed and solder bridges must be placed at the far end of the XTAL oscillator output traces as shown in Figure 1.
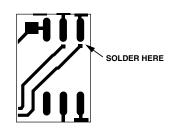


*Figure 1. Place Required Solder Bridges at End of Traces (Under the LVEL16 Part)*
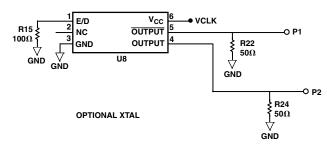


*Figure 2. Schematic Using the Vectron JN00158 XTAL*

The Vectron XTAL schematic is shown in Figure 2. To use the Vectron oscillator, remove the LVEL16, R19, and R20 from the board and connect the solder bridges as shown in

Figure 1. Place two 50 Ω (R22, R24) terminations to ground at the outputs of the XTAL. The Enable pin on the XTAL should be connected by placing a 100 Ω resistor to ground (R15). Figure 4 shows the final configuration of the board. Power for the crystal is supplied using the VCLK_VXTAL pin on the power terminal block. Place a 0.1 μF capacitor for C14. R38, R21, and R23 are not needed for this XTAL.
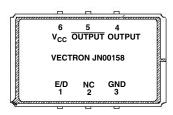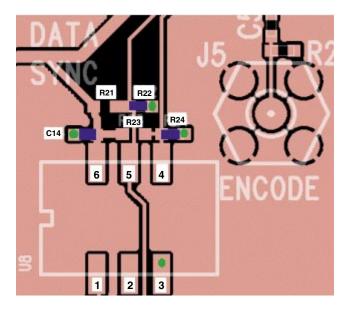


*Figure 3. Vectron XTAL Pinout*
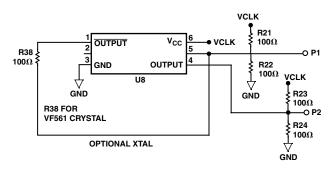


*Figure 4. Board Layout of the Vectron XTAL*

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Figure 5.  Schematic Using the Valpey-Fisher VF561

**XTAL USING THE VALPEY-FISHER XTAL**

The Valpey-Fisher schematic is shown in Figure 5. To use the Valpey-Fisher oscillator, remove the LVEL16, R19, and R20 from the board and connect the solder bridges as shown in Figure 1. R21, R22, R23, and R24 values can be adjusted to maintain a 50 Ω Thevenin equivalent termination to VCLK-2V if desired. (The outputs are ac-coupled at the ADC clock inputs.)

Place a 0 Ω or short across R38 for VO–. Figure 7 shows the final configuration of the board. Power for the crystal is supplied using the VCLK_VXTAL pin on the power terminal block. Place a 0.1 µF capacitor for C14. R15 is not needed for this XTAL.

The VF561 is available in a wide range of frequencies (15 MHz to 300 MHz) allowing for a variety of sample rates to be used and characterized. The low jitter (1 ps rms max) is sufficient to meet the AD9430 clocking requirements in most applications.
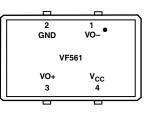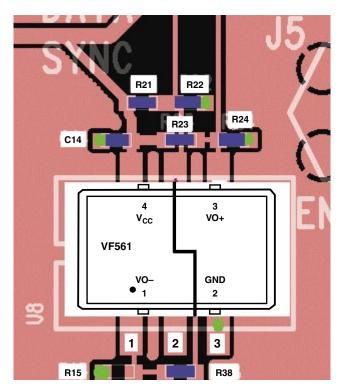


Figure 6.  Valpey-Fisher VF561 Pinout



Figure 7.  Board Layout of the Valpey-Fisher VF561

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