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APPLICATION NOTE

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Determining the Maximum Tolerable Frequency Drift Rate of the AD9548 System Clock in Low Loop Bandwidth Applications

by Ken Gentile

INTRODUCTION

The AD9548 is a digital PLL with a direct digital synthesizer (DDS) as a surrogate for the VCO that appears in an analog PLL. Unlike a VCO, however, the output signal of a DDS derives from a dedicated external clock source—the system clock. The system clock is essentially the sampling clock for the DDS.

The frequency of the system clock (f_S) relates to the DDS output frequency (f_O) via a digital frequency tuning word (FTW) as follows:

$$f_O = f_S \frac{FTW}{2^n} \quad (1)$$

where n is the number of bits in the DDS phase accumulator (n = 48 for the AD9548).

The AD9548 performs the PLL function by controlling FTW to produce the desired f_O in a manner similar to the way an analog PLL varies the VCO control voltage to produce the desired VCO output frequency.

In most applications, the stability of the frequency source (the VCO in an analog PLL or the system clock in the case of the AD9548) is not of primary concern because the action of the PLL control loop tends to compensate for any intrinsic frequency drift. In applications involving a very low loop bandwidth, however, the rate of frequency drift becomes an issue because the loop may not be able to respond quickly enough to compensate when the frequency drift rate is too high. The result is a shift in phase at the output of the PLL, which can be detrimental in some critical timing applications.

One such timing application is synchronization to a 1 pps global positioning system (GPS) reference signal. These applications require loop bandwidths in the 0.02 Hz range. With such a low loop bandwidth, the intrinsic frequency drift rate of the AD9548 system clock can result in the device losing lock. This raises the question: What intrinsic frequency drift rate associated with the system clock can the AD9548 PLL tolerate without causing an adverse effect? The purpose of this application note is to provide an answer to this question.

TABLE OF CONTENTS

REVISION HISTORY

8/10—Revision 0: Initial Version

FREQUENCY DRIFT ANALYSIS

VCO AND DDS FREQUENCY DRIFT MODELS

Because this application note focuses on the effect of system clock drift on the closed-loop operation of the AD9548 digital PLL, it makes sense to derive a model of frequency drift in an analog PLL vs. a DDS-based PLL. In an analog PLL (see Figure 1), the frequency source is a VCO. In a DDS-based PLL (see Figure 2), the frequency source is a fixed-frequency (f_S) external oscillator.

A VCO consists of a free running oscillator that oscillates at a given nominal frequency, f_C. However, the VCO is tunable over a frequency range, usually by means of a dc control voltage, V_C. A model of the VCO (see Figure 1) includes the nominal frequency source, which provides the base frequency (f_C), and an additional voltage-dependent frequency source associated with the frequency tunable component of the VCO. The tuning component provides a frequency offset that depends on the VCO gain (K_V). Therefore, the VCO output frequency (f_O) is the sum of the base and offset frequencies. Frequency drift at the VCO output (Δf_O) can result from oscillator drift (Δf_C), control drift (ΔK_V), or a combination thereof.

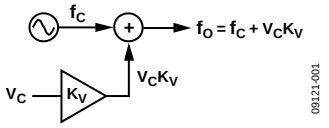

Figure 1. VCO Model

A DDS, on the other hand, relies on an external fixed-frequency oscillator clock source that serves as the DDS sample clock and operates at a frequency of f_S. A DDS model (see Figure 2) includes an input for the external sample clock, a control input (FTW) for frequency tuning, and a frequency gain element (K_X).

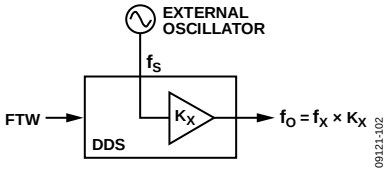

Figure 2. DDS Model

Normally, a DDS operates under the assumption that the external sample clock frequency, f_S, is a constant, stable frequency source. In this case, f_X and K_X in Figure 2 correspond to FTW and $f_S/2^n$ in Equation 1, respectively. That is, the output frequency changes proportionally to FTW according to the frequency gain factor, $K_X = f_S/2^n$.

Conversely, in the case of a nonconstant frequency source (one that exhibits drift), the previous assumption is no longer valid. Therefore, to analyze the effect of a nonconstant frequency source, assume FTW is constant. Then, f_X and K_X in Figure 2 correspond to f_S and $FTW/2^n$ in Equation 1, respectively. That is, the output frequency changes proportionally to f_S according to the frequency gain factor, $K_X = FTW/2^n$. However, Equation 1 indicates $FTW/2^n = f_O/f_S$, which leads to Equation 2 implying that changes in f_S translate to the output with a gain factor that is dependent upon the output frequency, f_O.

$$K_X = f_O/f_S \quad (2)$$

where:
f_O is the DDS output frequency for a given FTW.
f_S is the nominal drift-free sample clock frequency.

In summary, the value of the frequency gain element in Figure 2 depends on which input causes the output frequency to change. When FTW is the source of interest, then $K_X = f_S/2^n$. On the other hand, when f_S is the source of interest, then $K_X = f_O/f_S$.

S-DOMAIN LOOP MODEL

Although the AD9548 is a digital PLL, the usual s-domain analysis found in the literature for analog PLLs is still applicable. Consider the block diagram in Figure 3, which is an s-domain model of the AD9548 when operating in a closed-loop configuration. A description of the various building blocks follows.

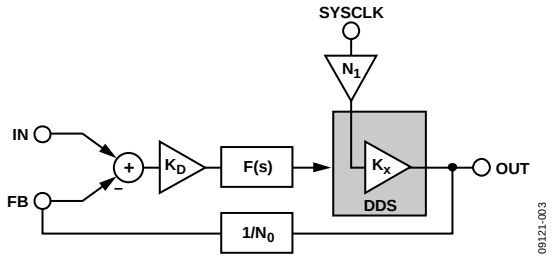

Figure 3. AD9548 s-Domain Block Diagram

There are four terminals associated with the closed-loop configuration: IN, FB, OUT, and SYSCLK. The IN terminal constitutes the reference input signal to the phase detector of the digital PLL, while the FB terminal constitutes the feedback input. Note the negative sign at the summing junction associated with the FB input, which indicates that the feedback signal subtracts from the input signal. The OUT terminal constitutes the output of the PLL (that is, the output of the DDS in the case of the AD9548). The SYSCLK terminal is where the user connects an external clock signal, which constitutes the source of the sample clock for the DDS.

The AD9548 provides the option of multiplying the SYSCLK input frequency via an integrated system clock multiplier PLL, which is a conventional analog PLL. The scale factor, N_1, in Figure 3 models the frequency multiplication effect of the system clock multiplier PLL. Although not shown explicitly in Figure 3, the system clock multiplier PLL includes a feedback divider (N), an input divider (M), and a 2× input frequency multiplier. The configuration of the system clock multiplier PLL is user programmable, which means that the value of N_1 depends on the user-defined configuration according to Table 1.

Table 1. System Clock Multiplier Scale Factor (N_1)

N_1	AD9548 System Clock Multiplier Configuration
1	Bypassed
N/M	HF path
N	LF or XTAL path, 2× multiplier bypassed
2N	LF or XTAL path, 2× multiplier enabled

Note that the digital PLL shown in Figure 3 includes a feedback divider ($1/N_0$) that divides the frequency at the OUT terminal by a factor of N_0 and delivers it to the FB terminal. The value of N_0 is variable because it is a user-programmable quantity. The digital PLL also includes a phase detector with Gain K_D, a loop filter with Transfer Function F(s), and a DDS with Gain K_X. In keeping with the s-domain model for the gain of the VCO in an analog PLL, the DDS gain from the output of the loop filter to the DDS output is K_X/s, where K_X is the tuning gain ($f_S/2^n$) and the 1/s term is the Laplace operator for integration.

RESPONSE TO A LINEAR FREQUENCY RAMP

According to Gardner (see the References section), the transient behavior of a Type II second order PLL is also applicable to Type II PLLs beyond second order. The AD9548 is a Type II fourth-order PLL; therefore, according to Gardner's premise, the transient behavior of a Type II second-order PLL still applies to the AD9548 even though it incorporates a fourth-order loop.

With this in mind, consider the response of a Type II second-order PLL to a linear frequency ramp at its input as shown in Figure 4. The frequency ramp has a constant slope of β (rad/sec^2). The steady-state condition for a Type II second-order PLL that results from the application of a linear frequency ramp at the IN terminal is a static phase error (θ_e) between the IN and FB terminals.

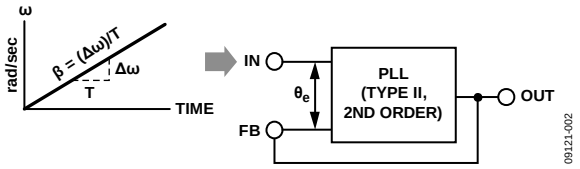

Figure 4. Linear Frequency Ramp Input

The static phase error resulting from an input frequency ramp is deterministic. It relates to the linear rate of frequency change (β) and the natural frequency (ω_n) of the second-order loop as shown in Equation 3.

$$\theta_e(\omega_n)^2 = \beta \quad (3)$$

Equation 3 requires θ_e to have radian units. However, it is often more desirable to refer to a time offset rather than a radian phase offset, but this requires knowledge of the nominal frequency (f_R) at the IN terminal. Given f_R, use Equation 4 to convert a time offset to a phase offset.

$$\theta_e = 2\pi f_R \Delta t \quad (4)$$

The significance of Equation 3 is that it relates a frequency ramp rate (β) at the IN terminal to a static phase offset (θ_e) given the natural frequency (ω_n) of the loop. If a way exists to relate β at the IN terminal to the SYSCLK terminal instead, then it should lead to a method for determining the maximum tolerable linear frequency drift of the system clock source. In fact, such a relationship exists as explained in the Relating a Frequency Ramp at the IN Terminal to the SYSCLK Terminal section.

NATURAL FREQUENCY

An obstacle to applying Equation 3 is the fact that the concept of natural frequency only applies to a second-order loop (a Type II PLL with a first-order loop filter, for example). This poses a problem because the AD9548 is a Type II PLL with a third-order loop filter (making it a fourth-order loop). Gardner, however, provides a means to extend the concept of natural frequency to Type II PLLs of an order greater than 2. This extension makes use of Equation 5.

$$\omega_n = \sqrt{\frac{K}{\tau_2}} \quad (5)$$

where:
K is the open-loop gain.
τ_2 is the time constant associated with the zero in the open-loop transfer function.

MAXIMUM TOLERABLE FREQUENCY RAMP AT THE IN TERMINAL

According to Equation 3, the frequency ramp rate (β) at the IN terminal (see Figure 4) depends on ω_n and θ_e. Because ω_n relates to the characteristics of the loop (K and τ_2 per Equation 5), its value is constant for a given PLL. On the other hand, θ_e depends on the slope (β) of the frequency ramp applied to the input of a Type II second-order PLL (see the Response to a Linear Frequency Ramp section). Therefore, choosing a maximum tolerable static phase offset at the input (θ_e) with ω_n being constant establishes the maximum tolerable frequency ramp (β) at the input via Equation 3. Furthermore, Equation 4 provides a means to express θ_e as a time offset rather than a phase offset.

For example, consider a maximum acceptable time offset of 10 ns (Δt = 10 ns), a nominal input frequency of 1 MHz (f_R = 1 MHz), and a loop natural frequency of 10 Hz ($\omega_n = 20\pi$ rad/sec). These values result in θ_e = 0.06283 rad (Equation 4) and β = 39.5 Hz/sec (see Equation 3). The value given for β requires dividing the result for β in Equation 3 by 2π to convert from rad/sec^2 to Hz/sec. This result implies that as long as the input frequency changes at a linear rate less than 39.5 Hz/sec, the time offset between the IN and FB terminals remains less than 10 ns.

Of course, application of Equation 3 requires a value for ω_n, something that has not yet been addressed. However, Equation 5 reveals that ω_n depends on K and τ_2, both of which relate to the characteristics of the loop filter. Fortunately, it is possible to determine K and τ_2 for the AD9548 loop filter as explained in the Determining the Natural Frequency of the AD9548 Loop Filter section.

RELATING A FREQUENCY RAMP AT THE IN TERMINAL TO THE SYSCLK TERMINAL

At this point, β (the maximum tolerable input frequency ramp rate) is quantifiable by specifying the amount of static phase (or time) offset one is willing to accept at the input (assuming one has a value for ω_n). However, the goal is to determine the maximum tolerable frequency ramp at the SYSCLK terminal, not at the IN terminal. Therefore, a means of relating a frequency ramp at the IN terminal to a frequency ramp at the SYSCLK terminal must be established.

Relating a frequency ramp at the IN terminal to a frequency ramp at the SYSCLK terminal first requires a more detailed explanation of what happens within the PLL for the following two different stimuli:

- A frequency ramp at the IN terminal (see Figure 5)
- A frequency ramp at the SYSCLK terminal (see Figure 6)

In both Figure 5 and Figure 6, the shaded rectangles are plots of frequency vs. time at various nodes in the loop, with blue denoting a stimulus signal and gray a response signal.

With a frequency ramp as the stimulus to the IN terminal (see Figure 5), note the stimulus at the SYSCLK terminal, which indicates a horizontal line (a slope of 0). This denotes a constant input frequency at the SYSCLK terminal, exactly what is expected for the system clock source. The constant frequency at the SYSCLK terminal results in a constant frequency at the output of the N_1 block (the equivalent of f_S in Figure 2).

The stimulus at the IN terminal is a frequency ramp with a positive slope of β, indicating a linearly increasing frequency over time. The equilibrium condition of the loop with a linear ramp at the IN terminal is a constant phase offset (θ_e) between the IN and FB terminals (see the Response to a Linear Frequency Ramp section).

The constant phase offset at the input of the phase detector causes a linearly increasing sequence of frequency tuning words at the output of the loop filter. Recall that the AD9548 is a digital PLL using numeric FTWs to control the output frequency of a DDS rather than a dc voltage to control the output frequency of a VCO. Therefore, the linearly ramping FTWs produce a linear frequency ramp at the OUT terminal.

The slope of the output ramp is such that it causes a replica of the ramp at the IN terminal to appear at the FB terminal (with a constant time offset defined by θ_e). The replicated ramp at the FB terminal is a necessary condition for equilibrium. Because the slope of the ramp at the FB terminal is β, the slope of the ramp at the OUT terminal must be βN_0 due to the feedback divider. The DDS, however, has a gain of $K_X = f_S/2^n$ associated with its control input. Therefore, the slope of the DDS control signal necessary to produce the ramp at the OUT terminal is the slope of the ramp at the OUT terminal divided by K_X as given by Equation 6.

$$Control\ Ramp\ Slope = \beta N_0/K_X = \beta N_0/(f_S/2^n) \quad (6)$$

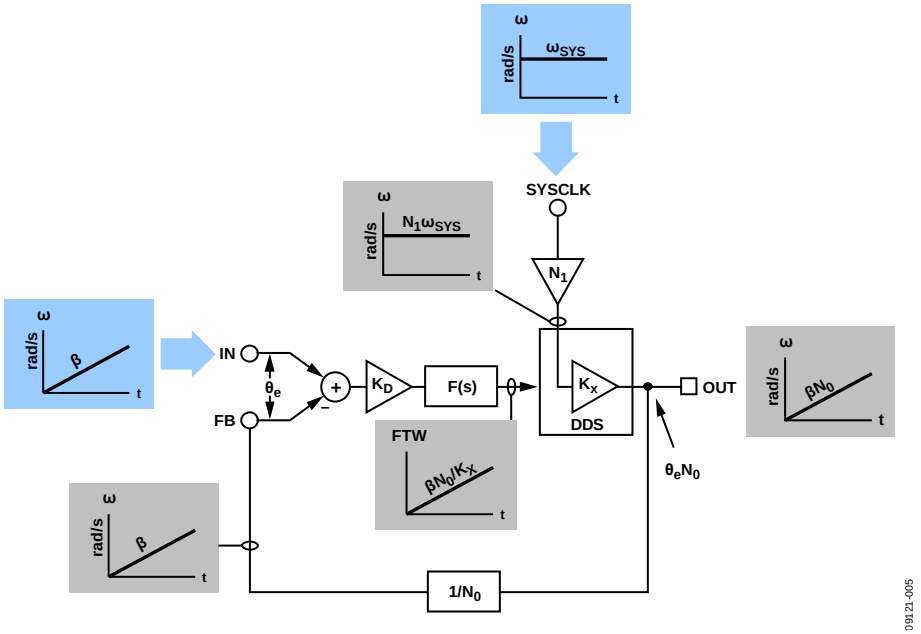

Figure 5. Frequency Ramp at the IN Terminal

Next, consider a frequency ramp stimulus at the SYSCLK terminal (instead of the IN terminal) as shown in Figure 6. Note the stimulus at the IN terminal, however, which indicates a horizontal line (a slope of 0). This constitutes a constant frequency at the IN terminal. In this case, a constant frequency at the IN terminal is necessary to clearly demonstrate how the loop responds to a frequency ramp stimulus at the SYSCLK terminal.

The stimulus at the SYSCLK terminal is a frequency ramp with a positive slope of β_{SYS}, indicating a linearly increasing frequency over time. The optional system clock multiplier PLL scales the slope by a factor of N_1 (see Table 1). If the loop is artificially broken at the connection between the loop filter and the DDS (simulating open-loop operation), the output signal becomes a frequency ramp with a slope of $\beta_{SYS} \times N_1 \times K_X$, where K_X is the DDS gain associated with its sample clock input according to Equation 2. Thus, in open-loop operation, the slope of the ramp at the OUT terminal is $\beta_{SYS} \times N_1 \times f_O/f_S$.

However, the fact that Figure 6 constitutes a closed loop with negative feedback means that the signal at the FB terminal must be the same as the signal at the IN terminal (a necessary condition for equilibrium). Therefore, both the IN and FB signals are a constant frequency. Furthermore, a constant frequency at the FB terminal requires a constant frequency at the OUT terminal (although scaled by the feedback divider).

To have a constant frequency at the OUT terminal, however, the control signal applied to the DDS must be a ramp with a negative slope (–α in Figure 6). In fact, the negative slope of the control signal ramp must be such that it counteracts the ramp at the output of the N_1 block to yield the required constant frequency at the OUT terminal. Note that a negative sloping control signal is only possible when a constant phase offset (θ_e) appears between the IN and FB terminals—the equilibrium condition of a PLL in response to a frequency ramp stimulus (see the Response to a Linear Frequency Ramp section).

Recall that in open-loop operation, the DDS output signal exhibits a frequency ramp with a slope of $\beta_{SYS} \times N_1 \times f_O/f_S$. To counteract this slope, however, the control signal must operate through the FTW input of the DDS, which has a gain of $K_X = f_S/2^n$. That is, α must equal the open-loop output slope ($\beta_{SYS} \times N_1 \times f_O/f_S$) divided by K_X per Equation 7.

$$\textit{Control Ramp Slope} = -(\beta_{SYS}N_1 f_O/f_S)/K_X$$
$$= -(\beta_{SYS}N_1 f_O/f_S)/(f_S/2^n) \quad (7)$$

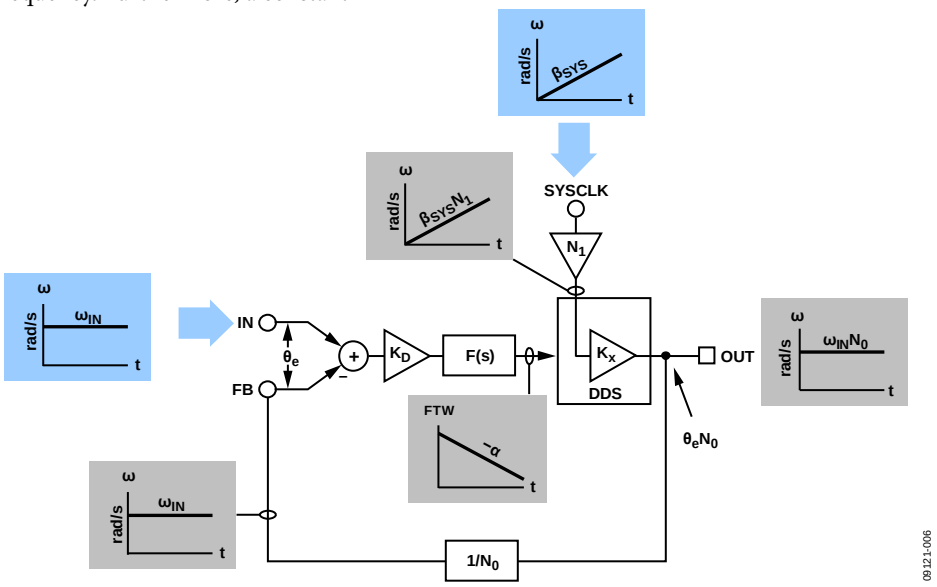

Figure 6. Frequency Ramp at the SYSCLK Terminal

Figure 5 and Figure 6 reveal that application of a frequency ramp at the IN or SYSCLK terminal results in a pair of matching signals at the IN and FB terminals with a static phase offset (θ_e) between them. Furthermore, to achieve equivalence between Figure 5 and Figure 6 requires θ_e to be the same magnitude in both cases. This provides a link between β and β_{SYS} via the DDS control signal. Thus, equating the magnitudes of the control ramp slopes (Equation 6 and Equation 7) establishes the necessary relationship between β and β_{SYS}.

$$| \beta N_0/(f_S/2^n) | = | - (\beta_{SYS} N_1 f_O/f_S)/(f_S/2^n) |$$

Solving for β_{SYS} yields

$$\beta_{SYS} = \beta(N_0/N_1)/(f_O/f_S) \quad (8)$$

In Equation 8, the default units for β_{SYS} are rad/sec^2. To convert to the more familiar units of Hz/sec, use Equation 9.

$$\beta_{SYS}\ (\text{Hz/sec}) = \frac{\beta_{SYS}}{2\pi} \quad (9)$$

Sometimes a normalized representation, like parts per million per second (ppm/sec), is more appropriate. Use Equation 10 to make the conversion.

$$\beta_{SYS}\ (ppm/sec) = \left(\frac{\beta_{SYS}}{2\pi}\right)\left(\frac{10^6}{f_{SYSCLK}}\right) \quad (10)$$

where f_{SYSCLK} is the nominal frequency of the source connected to the SYSCLK terminal (see Figure 3).

DETERMINING THE NATURAL FREQUENCY OF THE AD9548 LOOP FILTER

Calculation of Equation 8 requires a value for β, but this, in turn, requires a value for the natural frequency of the loop (ω_n) per Equation 3. Furthermore, determining a value for ω_n requires knowledge of the loop filter response. In the case of the AD9548, the loop filter is a digital filter with programmable coefficients, which gives the user control over the frequency response of the loop. Because the programmed coefficients determine the loop filter response, they also determine ω_n (the natural frequency of the loop).

The challenge at hand is to find a relationship between the filter coefficients and the parameters K and τ_2 in Equation 5, which allows calculation of ω_n. Then, substituting ω_n into Equation 3 enables calculation of β, which leads to β_{SYS} via Equation 8 (the maximum tolerable frequency drift rate of the system clock source).

The first step, however, is finding values for K and τ_2, which depend on the filter response as dictated by the loop filter coefficients. The standard design procedure for calculating the AD9548 loop filter coefficients involves the six design parameters in Table 2. Note that the feedback division factor (N_0) comprises an integer part, S, and an optional fractional part, U/V. Thus, the total feedback division value is S + U/V.

Table 2. Design Parameters

Parameter	Description
f_S	DDS sample rate (Hz)
f_C	Desired loop bandwidth (Hz)
θ_{PM}	Desired phase margin
f_3	Frequency offset (Hz), relative to the PLL output frequency, at which the third pole response yields additional attenuation, A
A	Additional attenuation (dB) of the third pole response at the offset frequency, f_3
N_0	Feedback division factor

The six parameters in Table 2 along with the two gain terms, K_D and K_V, allow for the computation of nine intermediate variables. These intermediate variables not only lead to the filter coefficients but also allow for the computation of K and τ_2, which are necessary for Equation 5. The two gain terms, nine intermediate variables, and associated formulas follow:

$$K_D = 10^{15}$$

$$K_V = \frac{f_S}{2^{48}}$$

$$\tau_1 = \frac{1-\sin(\theta_{PM})}{2\pi f_C \cos(\theta_{PM})}$$

$$\tau_3 = \frac{\sqrt{10^{\frac{A}{20}} - 1}}{2\pi f_3}$$

$$\tau_S = \tau_1 + \tau_3$$

$$\tau_P = \tau_1 \tau_3$$

$$\omega_0 = \frac{\tau_S \tan(\theta_{PM})}{\tau_P + \tau_S^2}\left(\sqrt{1 + \frac{\tau_P + \tau_S^2}{(\tau_S \tan(\theta_{PM}))^2}} - 1\right)$$

$$\tau_2 = \frac{1}{\omega_0^2 \tau_S}$$

$$C_1 = \frac{\tau_1 K_D K_V}{\omega_0^2 \tau_2 N_0}\sqrt{\frac{1+(\tau_2\omega_0)^2}{[1+(\tau_1\omega_0)^2][1+(\tau_3\omega_0)^2]}}$$

$$C_2 = C_1\left(\frac{\tau_2}{\tau_1} - 1\right)$$

$$R_2 = \frac{\tau_2}{C_2}$$

For the AD9548, the loop gain K (which is necessary to calculate ω_n per Equation 5) relates to K_D, K_V, N_0, C_1, C_2, and R_2 as follows:

$$K = \frac{K_D K_V C_2 R_2}{N_0 (C_1 + C_2)}$$

Note, however, that the equation for R_2 indicates τ_2 can replace C_2R_2 in the above equation for K. According to Equation 5, this means ω_n is expressible in terms of K_D, K_V, N_0, C_1, and C_2. However, C_2 is proportional to C_1, and the appropriate substitutions yield an alternate form for ω_n according to Equation 11. The significance of Equation 11 is ω_n (and by inference β) is independent of K_D, K_V, and N_0. However, Equation 11 involves ω_0, τ_1, and τ_3, implying that ω_n is dependent on θ_{PM}, f_C, f_3, and A (see Table 2).

$$\omega_n = \omega_0 \sqrt{\tau_S \omega_0 \sqrt{\frac{\left(1+(\tau_1\omega_0)^2\right)\left(1+(\tau_3\omega_0)^2\right)}{1+(\tau_S\omega_0)^2}}} \quad (11)$$

In summary, four of the six design parameters in Table 2 lead to the natural frequency (ω_n) of the loop for the AD9548 via Equation 11. Insertion of ω_n into Equation 3, along with the maximum acceptable phase offset (θ_e), yields the maximum tolerable frequency ramp rate (β) at the IN terminal. Then, β leads directly to β_{SYS} (via Equation 8), which is the maximum tolerable frequency ramp rate at the SYSCLK terminal for a given maximum acceptable phase offset (θ_e) between the IN and FB terminals.

AN ILLUSTRATIVE EXAMPLE

Consider the AD9548 configured as follows:

1. The reference input is a 1 Hz signal with the AD9548 input divider set to unity, resulting in a 1 Hz signal at the input to the phase detector (the IN terminal in Figure 3). Therefore,
   - f_R = 1 Hz
2. The AD9548 SYSCLK input (the SYSCLK terminal in Figure 3) is a 25 MHz oscillator and uses the HF path of the integrated system clock multiplier PLL (see Table 1.) to generate a 1 GHz system clock. Therefore,
   - f_{SYSCLK} = 25 MHz
   - N_1 = 40 (N_1 = N/M, where N = 40 and M = 1)
   - f_S = 1 GHz
3. With the AD9548 in closed-loop operation, the DDS output frequency is (155,520,000 + 185/188) MHz. Therefore,
   - S = 155,520,000
   - U = 185
   - V = 188
   - N_0 = S + U/V = 155,520,000 + 185/188
   - f_O = (155,520,000 + 185/188) Hz (because $f_O = f_R \times N_0$)
4. The loop filter has the following parameters (see Table 2):
   - f_C = 0.02 Hz
   - θ_{PM} = 60°
   - f_3 = 1 Hz
   - A = 15 dB
5. The maximum acceptable time offset at the phase detector input (the IN and FB terminals in Figure 3) is 1 ns. Therefore,
   - Δt = 1 ns

These parameters yield

$\tau_1 = 2.13227$

$\tau_3 = 8.80729 \times 10^{-1}$

$\omega_0 = 8.77306 \times 10^{-2}$

The values of τ_1, τ_3, and ω_0 enable calculation of ω_n via Equation 11 (note $\tau_S = \tau_1 + \tau_3$).

$\omega_n = 4.47996 \times 10^{-2}$

Use Equation 4 to convert Δt to θ_e.

$\theta_e = 2\pi f_R \Delta t = 6.28319 \times 10^{-9}$

Use Equation 3 to calculate β from ω_n and θ_e.

$\beta = \theta_e(\omega_n)^2 = 1.26104 \times 10^{-11}$ (rad/sec^2)

Use Equation 8 to calculate β_{SYS}.

$\beta_{SYS} = \beta(N_0/N_1)/(f_O/f_S) = 3.15259 \times 10^{-4}$ (rad/sec^2)

Use Equation 9 and/or Equation 10 to convert to Hz/sec and/or ppm/sec.

β_{SYS} (Hz/sec) $= 5.02 \times 10^{-5}$

β_{SYS} (ppm/sec) $= 2.01 \times 10^{-6}$

The significance of this result cannot be overemphasized—the maximum rate of change of frequency at the SYSCLK terminal for this example is a mere 50 µHz/sec. Because the nominal SYSCLK frequency for this example is 25 MHz, 50 µHz/sec translates to 2 micro-ppm/sec or 2 milli-ppb/sec (ppb is parts per billion).

CHOOSING THE PROPER SYSCLK SOURCE

For the specific case given in the An Illustrative Example section, the maximum tolerable rate of change of frequency at the SYSCLK terminal is 2 milli-ppb/sec, which implies the need for an extremely stable SYSCLK source to maintain a time offset (Δt) of no more than 1 ns.

Consider a SYSCLK source, for example, consisting of a very high quality 25 MHz OCXO capable of providing temperature stability in the range of 2 ppb/°C. Suppose such an OCXO experiences a 10°C temperature change over the course of an hour. Assuming that the temperature change ($\delta T/\delta t$) is constant over the one-hour interval, the frequency shift is

2 ppb/°C × 10°C/hour = 5.6 milli-ppb/sec

This is 2.8 times greater than the 2 milli-ppb/sec maximum tolerable rate of change of frequency for the example given in the An Illustrative Example section. For that particular case, there are three ways to deal with this problem of an excessive frequency drift rate.

- Choose an environment that keeps the temperature change to about 3.5°C/hour (instead of 10°C/hour).

- Choose an OCXO with a temperature stability specification of no more than 0.7 ppb/°C.
- Increase θ_e or ω_n, or a combination of both, to increase β by a factor of 2.8, thereby increasing β_{SYS} to 5.6 milli-ppb/sec (commensurate with the OCXO drift rate).

Considering the third option, it may be possible to increase the Δt requirement from 1 ns to 2.8 ns because Δt equates to θ_e (Equation 4) and θ_e is directly proportional to β (Equation 3), which is directly proportional to β_{SYS} (Equation 8). However, if changing Δt is not feasible, ω_n could be increased instead.

This, however, is a much more difficult option for two reasons. First, rather than β being directly proportional to ω_n, it is proportional to its square. Second, ω_n depends on the loop filter response, which relates to the parameters in Table 2. This makes the relationship between ω_n and the loop filter response quite convoluted.

NORMALIZATION HELPS QUANTIFY SYSCLK STABILITY REQUIREMENT

As a guide to assist in choosing an appropriate SYSCLK source, Figure 7 and Figure 8 offer a link between acceptable time offset (Δt), open-loop bandwidth (f_C in Table 2), and the maximum tolerable frequency ramp at the SYSCLK terminal (β_{SYS}). Both figures cover a range of f_C from 0.001 Hz to 0.1 Hz with β_{SYS} given in normalized units of ppm/sec. The use of normalized units allows for more meaningful plots because it masks the effect of N_0, N_1, f_O, and f_S on β_{SYS} (see Equation 8).

To benefit from normalization, however, requires a constant attenuation factor (parameter A in Table 2). To this end, all plot traces are for A = 3 dB. Normalization also requires the offset frequency (parameter f_3 in Table 2) to scale with f_C by a constant factor, which is the case for all plot traces. However, to capture the effect of changing the relative position of f_3, each Δt value comprises two traces—a black trace corresponding to $f_3 = 10 \times f_C$ (a scale factor of 10) and a red trace corresponding to $f_3 = 20 \times f_C$ (a scale factor of 20).

Comparison of the two figures reveals that a particular Δt trace in Figure 7 ($\theta_{PM} = 50°$) results in a higher β_{SYS} value relative to the same Δt trace in Figure 8 ($\theta_{PM} = 80°$). This implies a less stringent stability requirement on the SYSCLK source for a lower θ_{PM} value. Furthermore, the separation between red and black traces for a given Δt value seems to indicate that higher θ_{PM} values are more sensitive to the location of f_3. For example, Figure 7 ($\theta_{PM} = 50°$) reveals about a 25% increase in β_{SYS} when scaling f_3 by a factor of 20 (red trace) vs. a factor of 10 (black trace). This suggests there is a slightly less stringent requirement on the stability of the SYSCLK source for f_3 scaled by 20 vs. 10 given $\theta_{PM} = 50°$. On the other hand, Figure 8 ($\theta_{PM} = 80°$) reveals about a 100% increase in β_{SYS} when scaling f_3 by a factor of 20 (red trace) vs. a factor of 10 (black trace). This implies a factor-of-two less stringent stability requirement on the SYSCLK source for f_3 scaled by 20 vs. 10 given $\theta_{PM} = 80°$.

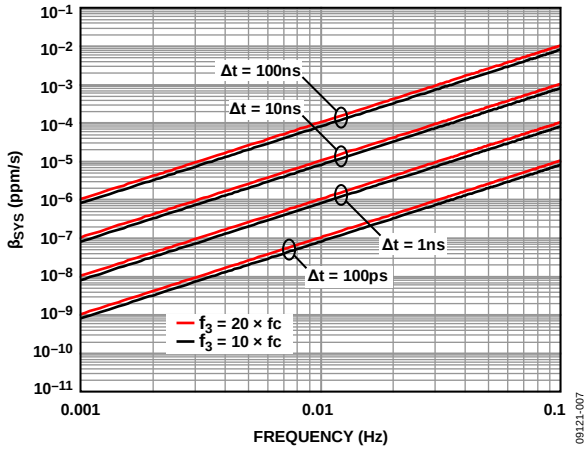

Figure 7. $\theta_{PM} = 50°$

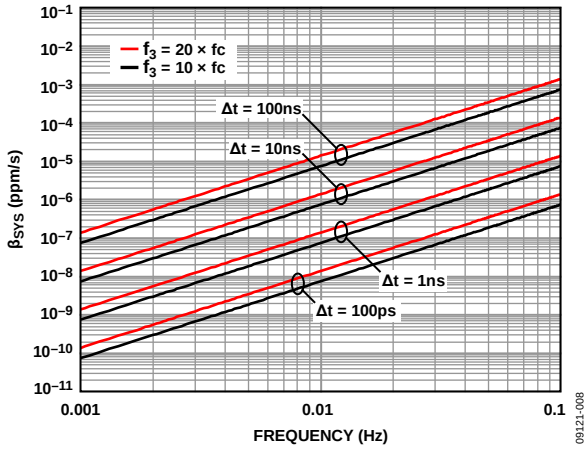

Figure 8. $\theta_{PM} = 80°$

CONCLUSION

Using the AD9548 to generate an output clock signal synchronized to a 1 pps GPS reference signal requires a very low loop bandwidth (0.02 Hz, for example). A very low loop bandwidth results in a similarly low natural frequency.

The low natural frequency combined with the requirement of a stringent time offset (Δt) leads to a very small value for β_{SYS} (the maximum tolerable rate of change in frequency at the SYSCLK terminal for which the loop can maintain a time offset of Δt or less). Finally, the very small β_{SYS} value implies the need for an extremely stable SYSCLK source. Thus, it requires great care in choosing the appropriate SYSCLK source when employing very narrow loop bandwidths.

METHODOLOGY CAVEATS

The method described herein for establishing a value for β and applying Equation 8 allows for quantifying β_{SYS}. The value of β_{SYS} represents the maximum rate of change of frequency at the SYSCLK terminal of the AD9548 that results in a phase (or time) offset of no more than θ_e (or Δt) given a particular device configuration.

Keep in mind that the maximum tolerable linear drift rate of frequency indicated by β_{SYS} relies on the following assumptions:

- The frequency drift is of constant slope ($\delta f/\delta t$ = constant) and persists long enough for the loop to reach equilibrium (steady-state condition).
- Using the s-domain model for an analog PLL is sufficiently accurate for modeling the behavior of the AD9548.
- The transient behavior of a second-order loop is sufficiently similar to that of higher order loops, which justifies the use of Equation 3.
- The extended definition of natural frequency, as proposed by Gardner, justifies the use of Equation 5.

The implication of these assumptions is that the calculated value of β_{SYS} is an estimate of the maximum tolerable frequency drift, rather than a hard boundary condition.

REGARDING THE LOOP BANDWIDTH OF THE SYSTEM CLOCK MULTIPLIER PLL

Some applications involve the use of the AD9548's integrated system clock multiplier PLL to translate a relatively low frequency SYSCLK source to a frequency high enough to accommodate the DDS. Such was the case demonstrated in the An Illustrative Example section. When the system clock multiplier PLL is in use, its bandwidth has a potential effect on a frequency ramp (β_{SYS}) appearing at the SYSCLK terminal. Fortunately, the bandwidth of the system clock multiplier PLL is so wide relative to the slow frequency ramps under consideration in this application note, the impact of its loop response on determining β_{SYS} is inconsequential.

REFERENCES

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NOTES

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