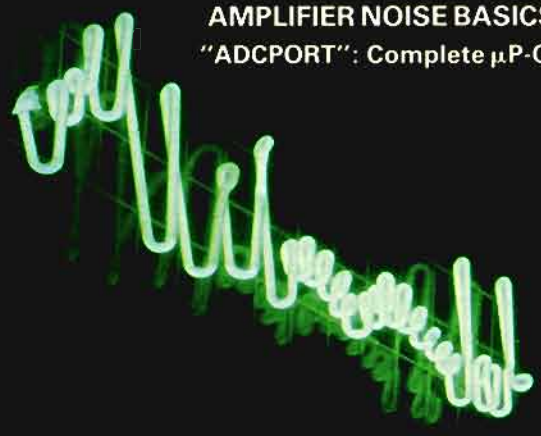
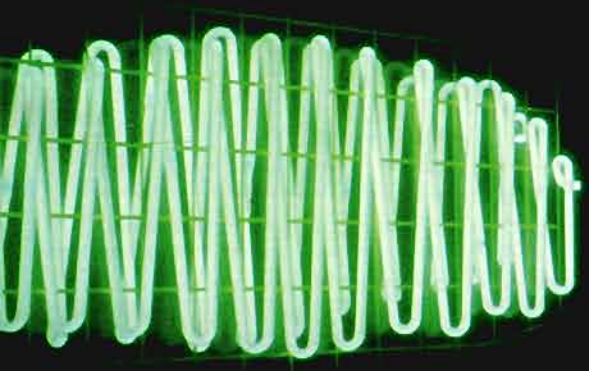
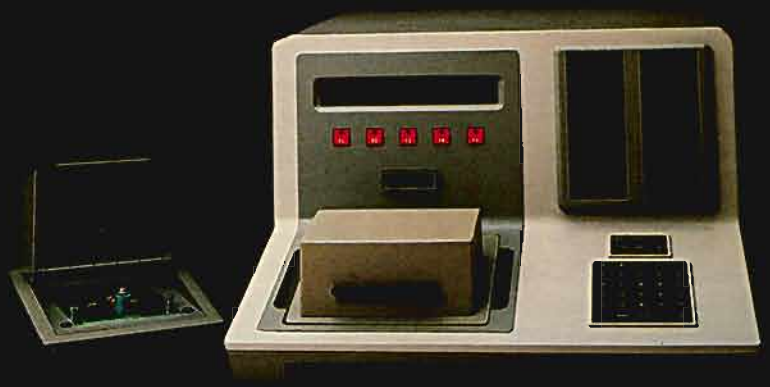
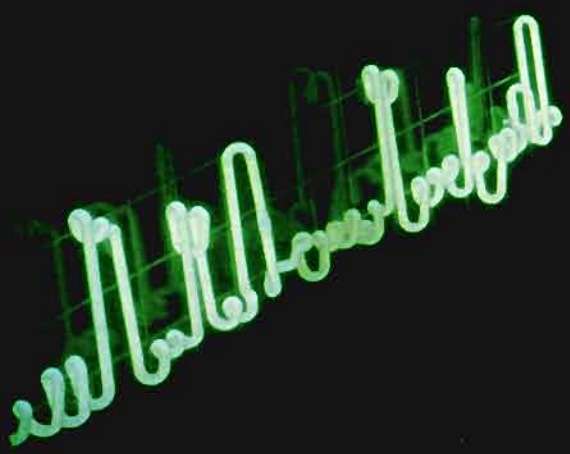
analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing









Volume 18, Number 1, 1984

ANALOG DEVICES

Editor's Notes

A SALUTE TO IEEE

In 1984, IEEE is celebrating its Centennial, as the successor organization formed by a merger in 1963 between the AIEE (American Institute of Electrical Engineers, founded in 1884) and the IRE (Institute of Radio Engineers, 1912).

Much that is important in today's electrotechnology was first proposed or reported on at IEEE-sponsored conferences and in IEEE publications. Most of the illustrious contributors to the recent history of electrotechnology, whose names are household words, were members of IEEE.

During the coming year, you will hear much of the history and statistics of IEEE and about its Centennial—in any medium you happen to be tuned in to. Indeed, it will be impossible to avoid.

So it is not necessary for us to recite endless historical details or reams of facts and statistics about the numbers of members (approaching a quarter-million), the number and magnitudes of Societies and Councils housed under IEEE's copious roof, the number of conferences held under its aegis, the truly back-breaking number of publications at all levels—in both serial and book form—the sweep of its grassroots technical and educational activities (in Sections around the world), its vital standards activity, and its decade-old (and steadily evolving) "professional" activities, under the banner of its U. S. Activities Board. Congratulations to IEEE on its 100th anniversary!

CONTRIBUTE BEFORE YOU COMPLAIN

In the electronics trade press, we see criticisms of IEEE, particularly in relation to its purported neglect of the "working engineer." We believe that criticism is beneficial; either because of it or in spite of it, IEEE is growing rapidly, is embracing change, and, in many ways, is as healthy as we have ever seen it.

Our (your Editor's) involvement with IEEE has included major elective Society office and appointive activity on headquarters committees and boards. However, our most treasured activity has centred on the ongoing grassroots program activities of an IEEE technical-Society chapter in the Boston Section. We have contributed to its technical program via down-to-earth technical talks at local meetings, organized a Lecture Series, and perenially served on the program committee, contributing and evaluating subject matter, and taking responsibility for organizing meetings.

As a working local volunteer, in contact with members and other volunteers on a practical technical organizational level, we have gotten tremendous pleasure from our IEEE connection—and an appreciation that without such activity IEEE would be of far less value to its members. True also of those other grassroots volunteers who organize and participate in conferences, and those who write—and review—papers. IEEE *is* its volunteers. We suggest that people not criticize or complain about what IEEE has or hasn't done for the "working engineer" until they've tried contributing (of) themselves through IEEE in some modest way for their fellow working engineers' benefit.

Dan Sheingold

THE AUTHORS

Donald W. Brockman (page 18) is Technical Communications Manager at ADI's Computer Labs Division (formerly Computer Labs Incorporated), which he joined in 1968 from Bell Telephone Laboratories. His formal education includes a B. A. degree and he has worked in engineering, writing, recruiting, and sales functions before his present job in Marketing.

Doug Grant (page 24), New-Product Marketing Manager for data converters at Analog Devices Semiconductor, gained substantial recognition as a Microcircuits Applications Engineer at ADS and has published numerous papers and articles. He has a BSEE from Lowell Technological Institute and extensive experience in developing converters, μP-based data-acquisition systems, and analytical instruments. He is also active in Amateur Radio.

Diane Heerema (page 24), a Marketing Engineer for converter products at Analog Devices Semiconductor Division, was graduated from Rutgers in 1979 with B.S. degrees in E.E. and Physiology. After a brief period at Exxon Enterprises (Battery Division) as an Applications Engineer, she became an Applications Engineer at ADI's System Components Division. She joined ADS in 1981.

Matt Johnson (page 14) is an applications engineer at the Analog Devices Digital Signal Processing Division (Norwood MA). He earned the BSEE degree at the Worcester Polytechnic Institute. Before joining ADI within the last two years, he worked at Teradyne, Inc., as a test engineer. Matt's leisure-time interests include speech synthesis, home computers, and music (jazz, bluegrass, and classical).

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2 Technology Way, P.O. Box 280, Norwood, Mass. 02062

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D-C AMPLIFIER NOISE REVISITED

Understanding, Measuring, and Testing for Random Noise

A New Op-Amp Noise Fixture for Automatic Benchtop Tests with LTS-2010

by Al Ryan and Tim Scranton

"Like diseases, noise is never eliminated, just prevented, cured, or endured, depending on its nature, seriousness, and the costs/difficulty of treating it."[1]

In Analog Dialogue *3-1 (1969)—now out of print—we published an article entitled "Noise and Operational Amplifier Circuits,"[2] intended to be a readable and easily applicable essay on noise principles, with primary emphasis on random noise, in a treatment distinguished more by vigor than by rigor[3]. On this, its 15th anniversary, it seems appropriate to review the salient tutorial, proffer data on modern IC op amps, and discuss the test means embodied in a new test socket assembly for automatic noise testing, employing the LTS-2000 family of benchtop device testers.*

WHY BE CONCERNED ABOUT NOISE?

An understanding of noise is needed to know what the real resolution of your system is. A knowledge of noise characterization and testing is needed to evaluate an amplifier or other purchased device with a given set of noise specifications.

As conversion systems employ increased digital resolution, the value of the least-significant bit decreases. For example, the LSB of a 10-bit system with 10V full scale is about 10 millivolts, the LSB of a 12-bit system is about 2.5 millivolts, and the LSB of 16 bits is 153 microvolts. This, by itself, poses significant problems in converter design.

However, the real-world measurement situation is worse, because most signals derived from real-world sources have full-scale amplitudes considerably less than 10 volts and must be amplified. If, for example, the original signal has a full-scale level of 10 mV (not unusual in transducer applications) and thus requires amplification of 1000×, the 12-bit LSB would become about 2.5 μV. If the preamplifier and its associated active and passive circuit elements generate only 1 μV of noise—or 100 pA in 10,000 ohms—(referred to the input) when the signal is sampled, they will significantly affect the accuracy, perhaps neutralizing the resolution.

Noise in data-acquisition systems takes three basic forms, *transmitted noise*—inherent in the received signal, *device noise*—generated within the devices used in data acquisition (preamps, resistors, etc.), and *induced noise*—picked up from the outside world, power supplies, logic, or other analog channels by magnetic, electrostatic, or galvanic coupling.

Transmitted noise must be dealt with, to the degree possible, by reducing noise at the source or in the transmission medium, and otherwise by making use of statistical analysis and filtering to distinguish between properties of the signal and of the noise, often employing techniques of digital signal processing (DSP).[4]

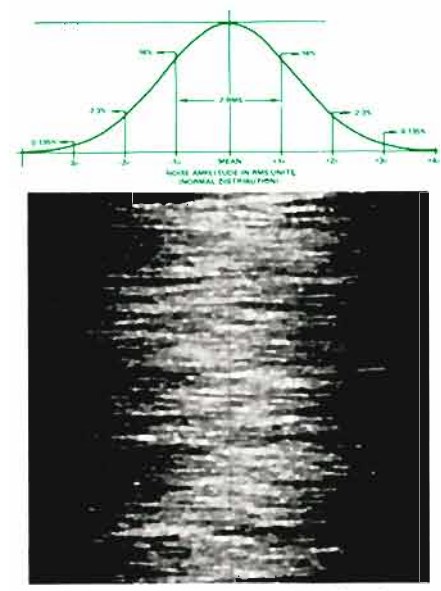

Figure 1. Gaussian amplitude distribution, juxtaposed against random-noise waveform.

Induced noise is affected by both electrical design choices and physical layout. Purposeful use of design techniques to predict and

[1] *Analog-Digital Conversion Notes*, ed. by D. H. Sheingold, Analog Devices, Inc., $5.95.

[2] Based on work done by L R. Smith at Analog Devices.

[3] A bibliography on random noise will be found on page 30.

[4] Good information and bibliographies on DSP can be found in articles recently published in *Analog Dialogue*: "CMOS ICs for Digital Signal Processing," (17-1, 1983) and "Digital FIR Filters without Tears" (17-2, 1983). Also available free from Analog Devices: "A Cookbook to Digital Filtering and Other DSP Applications," a collection of reprints of papers that originally appeared in EDN magazine during 1983.

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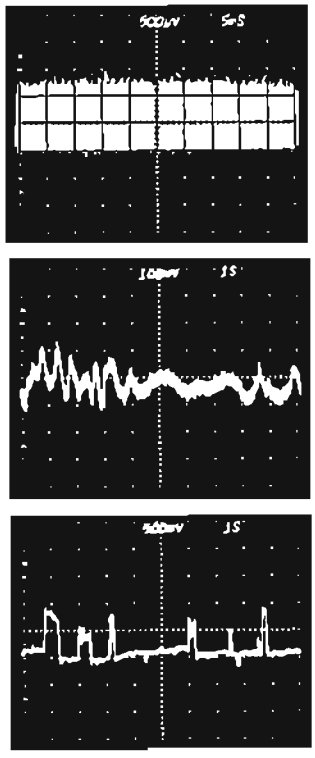
reduce induced noise was discussed in *Analog Dialogue* in a two-part series by Alan Rich.[5]

This article is about the irreducible minimum—*device noise*—its properties, how it affects circuit performance, and how it is measured. Later in the article, we will describe a test fixture that can be used for noise tests employing the Analog Devices LTS-2000 family of automatic benchtop testers.

RANDOM NOISE

Resistors and semiconductor junctions generate *random* noise: the output amplitude at a given instant is uncorrelated with the output amplitude at some other instant, and any value of output is possible at any instant—but it cannot be predicted. When a large number of samples are taken, many stationary random processes have amplitude distributions that appear *Gaussian*, i.e., characterized by the familiar bell-shaped curve (Figure 1). If the distribution is of voltages, and if care has been taken to eliminate dc offsets, then the rms voltage will be equal to the standard deviation of the distribution. Since random noise tends to be a stationary process,* the rms value tends to be constant for a given bandwidth and/or (sufficiently long) averaging interval.

Device-produced random noise, when plotted on an oscilloscope screen, can be identified in terms of several characteristic signatures. The noise output of a single device may combine all three types. Figure 2 (a) shows broad-spectrum "white" noise, which may be thermal (Johnson), or shot (Schottky); it has a constant distribution across the frequency spectrum but looks as if it is heavily oriented to the higher frequencies. Figure 2 (b) shows "pink", or "1/f", or "flicker" noise, dominated by low frequencies, and (c) illustrates "popcorn" noise (so-called because of its sound when presented audibly), characterized by random jumping between two or more levels.



(a) White noise.

(b) 1/f noise.

(c) Popcorn noise.

Figure 2. Noise signatures.

[5]"Understanding Interference-Type Noise," *Analog Dialogue 16-3*; and "Shielding and Guarding," *Analog Dialogue* 17-1

*The statistical properties of a stationary process are invariant under a shift of the time origin.

Since popcorn noise consists of jumps having approximately equal amplitudes, devices that have popcorn noise tend to have anomalous sharp peaks in the amplitude distribution, indicating that the number of such amplitudes greatly exceeds their probability in a purely random distribution.

White noise is present in all resistors and in semiconductor junctions. Resistor noise is thermal noise; its average power in a given bandwidth depends on temperature. Semiconductor junction noise is known as shot noise; its rms current variation in a given bandwidth is a function of the dc current through the junction.

"Excess noise" comprises all device noise that exceeds theoretical white-noise levels; it may be found when current flows through resistors, especially carbon composition types; it contains both shot noise and flicker components that are due to contact between carbon granules in resistors. For this reason, good practice mandates metal-film or wirewound resistors whenever low noise is required in the presence of significant dc current flow.

Flicker noise in semiconductors is due to random fluctuations in the number of surface recombinations; and "popcorn noise," a negative indicator of semiconductor process quality, is due to random on/off recombination action in the semiconductor material, leading to erratic switching of an affected device's current gain.

QUANTITATIVE MEASURES

The average *Johnson noise power*, generated by thermal agitation of the electrons in a resistor, and dissipated in a circuit containing a matched resistive load of equal magnitude is given by (1):

$$P_n = k\,T\,B \text{ watts} \qquad (1)$$

where

k = Boltzmann's Constant = 1.381×10^{-23} joules/kelvin

T = Absolute temperature, kelvins (°C + 273.2°)

B = Bandwidth, $f_2 - f_1$, ("brick wall"*) in hertz.

In a series circuit with a resistor, R, containing a noise generator, E_n, and a matched resistor, of value R, the power dissipated in the load resistor is $(E_n/2)^2/R$, therefore

$$E_n = \sqrt{4\,k\,T\,R\,B} \text{ volts} \qquad (2)$$

where E_n is the rms value of voltage generated in source resistance R. Near room temperature, and with more-convenient units (i.e., T = 300 K, and R × B in meg(ohm-Hz)

$$E_n = 0.129\sqrt{R \times B} \text{ microvolts rms} \qquad (3)$$

Example: if R = 1kΩ and B = (5 kHz − 4 kHz) = 1 kHz, E_n is equal to 0.129 μV. If R = 100Ω and B = 1 kHz, E_n = 41 nV.

Johnson noise is quite often expressed in terms of an equivalent current source, I_n, in parallel with the resistor,

$$I_n = E_n/R = 0.129\sqrt{\frac{B}{R}} \qquad (4)$$

where B is in hertz and R is in megohms.

Shot noise, caused by current flowing through a junction, is normally expressed as an ac current component, added to the dc value of I; it will produce voltage drops in series impedances, such as transistor emitter resistance or op-amp computing resistors:

$$I_n = \sqrt{2\,e\,I\,B} = 5.66 \times 10^{-10}\sqrt{I\,B} \text{ amperes rms} \qquad (5)$$

where

*Perfect sharp-cutoff filtering.

e = Unit charge, 1.602×10^{-19} coulombs
I = DC current flowing through the junction, amperes
B = Bandwidth, $f_2 - f_1$ hertz ("brick wall")

Expressed in more convenient units, if I is in microamperes,

$$I_n = 0.566\sqrt{I}B \text{ picoamperes} \quad (6)$$

NOISE DENSITY SPECTRUM

Noise exists in all parts of the frequency spectrum; the noise contribution of a resistor or amplifier varies with the bandwidth over which the observation is made. Characterization of noise in terms of its *spectral density*, i.e., as a function of frequency, makes calculation of noise in differing bandwidths in active circuits easier. A useful way of presenting noise characteristics graphically is via a plot of noise spectral density vs. frequency.

The power spectral density is defined as the derivative of noise power with respect to frequency (watts per hertz), i.e.,

$$p_n = \frac{dP_n}{df} \quad (7)$$

Since power is proportional to the square of rms voltage or current, the respective expressions for voltage and current noise spectral density are:

$$e_n = \sqrt{\frac{dE_n^2}{df}} \text{ and } i_n = \sqrt{\frac{dI_n^2}{df}} \quad (8)$$

with units of $V/\sqrt{Hz}$ and $A/\sqrt{Hz}$. Figure 3 shows typical spectral density plots of AD741 voltage and current noise, (a) and (b), compared with the low-noise bipolar AD OP-27's e_n and i_n (c) and the the low-drift FET-input AD547's e_n (d). Voltage noise tends to have a lower "corner" frequency (see 1/f noise, next page) than current noise in bipolar amplifiers. Illustrating different ways of presenting the data, the scales of (a) and (b) show mean-square voltage and current spectral density per hertz, while (c) and (d) show rms voltage and current spectral density per $\sqrt{Hz}$; (d) is a semilog plot with a linear voltage scale for greater sensitivity to small noise voltage changes in the vicinity of the corner frequency.

The rms voltage or current in a given frequency band is determined by integrating the expressions in (8), i.e.,

$$E_n [f_1 \text{ to } f_2] = \sqrt{\int_{f_1}^{f_2} e_n^2 df} \quad (9)$$

Spot Noise. If $f_2 - f_1$ is quite small, we can assume that e_n is essentially constant (or "white") in that band (or "spot"), and $E_n = e_n\sqrt{f_2 - f_1}$. Using this, we can derive noise spectral density from a series of narrow-band measurements; the individual values of e_n are $E_n/\sqrt{f_2 - f_1}$. Enough points are observed to define a curve. These measurements are not easy to make, especially at low frequencies. By the same token, we can integrate a spectral-density curve of any shape by dividing the spectrum into small enough increments and taking the root sum-of-squares of the individual rms spot-noise contributions.

Graphical integration can be used to good effect, because plotted data based on measurements is seldom describable by easy formulas, and bandwidths aren't "brick-wall." However, approximations are often available that make it unnecessary to perform actual integrations over wide ranges of the noise characteristic.

EXAMPLES OF SPECTRAL DENSITY

Some simple rules for calculating noise over any bandwidth can be ascertained by the examination of two common forms of noise, white noise and 1/f noise.

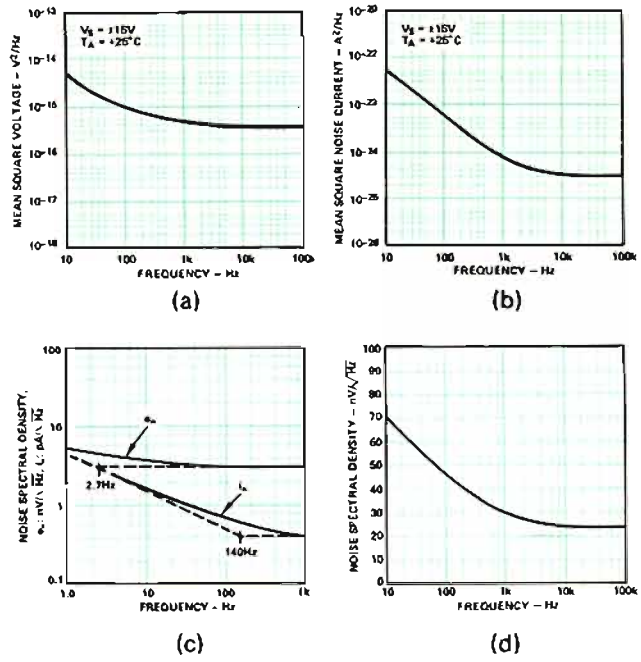


Figure 3. Noise spectral density plots. (a) Voltage-squared/Hz vs. frequency for AD741. (b) Amperes-squared/Hz vs. frequency for AD741, log-log plot. (c) Voltage and current per root hertz for AD OP-27, log-log plot. (d) Voltage per root hertz for AD547, semi-log plot.

White noise. As equations (1) and (5) show, white-noise power is of the form, (constant) × $(f_2 - f_1)$, which can be recognized as the definite integral of (constant) with respect to frequency between the limits of f_2 and f_1. For white noise, the spectral density is thus a theoretical or measured constant. Similarly, the voltage and current spectral densities, e_n and i_n, are equal to the square-roots of the respective constants ($0.129\sqrt{R}$ microvolts for Johnson voltage, $0.129/\sqrt{R}$ picoamperes for Johnson current (R in megohms), and $0.566\sqrt{I}$ picoamperes for shot current (I in μA). The right-hand portions of the graphs in Figure 3 illustrate the approximately constant level of white noise at the higher frequencies.

From the curves in the white noise regions, wideband noise for any bandwidth is easily calculated as the product of voltage or current spectral density and the square root of the bandwidth $(f_2 - f_1)$. For voltage noise, if e_n is given:

$$E_n = e_n \times \sqrt{f_2 - f_1} \quad (10a)$$

If $(e_n)^2$ is given,

$$E_n = \sqrt{(e_n)^2 \times (f_2 - f_1)} \quad (10b)$$

If $f_1 < 0.1\ f_2$, the error in assuming $f_2 - f_1 = f_2$ is less than 5%.

Example: Calculate the noise in the band, 100 Hz to 10 kHz, for each curve in Figure 3. The results are shown in the table:

Curve (Fig. 3)	Device	Quantity	Value from curve	Calc. rms noise
(a)	AD741	$(e_n)^2$	3.5×10^{-16} V²/Hz	1.86μV rms
(b)	AD741	$(i_n)^2$	3×10^{-25} A²/Hz	54 pA rms
(c)	AD OP-27	(e_n)	3×10^{-9} V/√Hz	0.3 μV rms
(c)	AD OP-27	(i_n)	0.4×10^{-12} A/√Hz	40 pA rms
(d)	AD547	(e_n)	23×10^{-9} V/√Hz	2.3 μV rms

Although the values of e_n and i_n are not strictly constant over the band, the value of wideband noise is always dominated by the higher frequency; if f_2 is well into the white-noise region, the shape of the curve at the lower frequencies will have negligible effect on *wideband* noise measurements.

Flicker noise, or "1/f" noise, has a noise power spectral density varying inversely with frequency. It is of the form (constant)/f^γ; γ may be any value from 0 to 2, but it is usually close to 1. The shape of the left-hand portion of the noise curves in Figure 3 is due to 1/f noise, and the asymptotic slope—on a log-log plot—at the lowest frequencies is determined by γ. The point at which the projected 1/f asymptote crosses the average white-noise spectral density is the "corner frequency;" it is a measure of the quality of the device process—better devices have lower corner frequencies.

For voltage (and correspondingly for current),

$$e_n = K\sqrt{\frac{1}{f}} \qquad (11)$$

K is the actual or extrapolated value of e_n at f = 1 Hz.

To compute E_n for the band, f_1 to f_2, using (9),

$$E_n(f_1 \text{ to } f_2) = K\sqrt{\int_{f_1}^{f_2} \frac{df}{f}}$$

$$= K\sqrt{\ln\left(\frac{f_2}{f_1}\right)} \qquad (12)$$

The important result here is that equal amounts of 1/f noise will be generated in frequency bands having equal ratios. Every octave ($f_2 = 2f_1$) or decade ($f_2 = 10f_1$) in the 1/f-noise region will generate as much noise as every other octave or decade (i.e., $0.83 \times K$ per octave and $1.52 \times K$ per decade);and the noise generated over *m* octaves or decades will be $\sqrt{m}$ times as great as that generated in a single octave or decade.

Consider, for example, the rms value of noise in the 9-decade realm below 1 Hz (down to about *1 cycle per 32 years*). If the rms value of noise in the decade, 0.1 Hz to 1.0 Hz, is 1 microvolt, then the noise over 9 decades will be $\sqrt{9} \times 1 = 3.0\ \mu V$! Over such long periods,—unless K increases—flicker noise can be expected to be less significant than drift caused by environmental factors, component aging, and perhaps even component life (however, there is evidence that increased 1/f noise—i.e., increased K—is often part of the end-of-life syndrome).

Example: What rms noise can be expected in the band, 0.1 to 10 Hz, for the devices plotted in Figure 3 (a), (b), and (c), extrapolating the curves to be asymptotic to a 1/f slope? The results are shown in the table.

Curve	K (Extrapolated)	Calculated E_n	Corner Frequency
(a)	$0.22\ \mu V/\sqrt{Hz}$	0.47 μV rms	100 Hz
(b)	$22\ pA/\sqrt{Hz}$	47 pA rms	2 kHz
(c) e_n	$4.9\ nV/\sqrt{Hz}$	12 nV rms (white)	2.7 Hz
i_n	$4.7\ pA/\sqrt{Hz}$	10 pA rms	140 Hz

Noise amplitude and Crest Factor. The rms value of noise is a consistent measure and is especially useful when dealing with signal phenomena having stationary properties, such as ac waveforms. However, in many cases, the accuracy or resolution of data is affected by the *instantaneous* value of noise, for example, sampled dc measurements and one-shot responses. For these, we must know the expected peak or peak-to-peak values of noise.

Although all values of noise amplitude are theoretically possible, there is a rapid decrease in the likelihood of large values, corresponding to the residual area under the distribution curve (Figure 4) beyond a given value. For example, the probability of a *crest factor* (peak/rms) exceeding 3.3 is 0.1%; for a c.f. exceeding 6, it is 2×10^{-9}. Figure 4 is a table and plot of the percentage of time that noise can be expected to exceed a given nominal peak-to-peak value (2 × c.f.), for a Gaussian distribution.

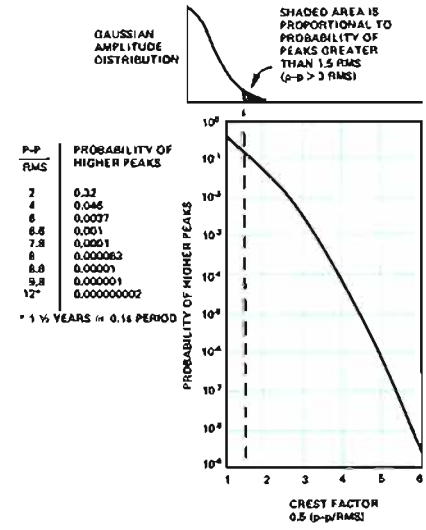


Figure 4. Crest factor of gaussian noise. For a measurement period of 0.1 seconds, a crest factor of 6 can be expected to occur once in 1 ½ years.

Combining noise. Noise from uncorrelated sources adds as the square-root of the sum of the squares of the individual rms values,

$$E_n = \sqrt{(E_{n1})^2 + (E_{n2})^2 + \ldots + (I_{n1}R_1)^2 + \ldots} \qquad (13)$$

Examples of uncorrelated sources are different resistors, transistors, diodes, amplifiers, etc. However, the magnitudes of the noise voltage and the current that it causes to flow through a resistor (or any impedance) are correlated.

Since noise values are random with time, they are also random with frequency; thus, it is reasonable to consider that rms noise in different "brick-wall" frequency bands is uncorrelated and may be combined in root-square fashion. In fact, the integral performs just that function, using infinitesimal bands and the "spot" value of spectral density at each. This suggests that, in the example of Figure 5, we can treat the total noise given by integrating the spectral distribution characteristic over the broad frequency range as the noise obtained by separately integrating over the numbered regions and vector-summing (root sum-of-squares) the results.

NOISE AND AMPLIFIERS

The model of a differential operational amplifier for noise, lumping the effects of all the internal sources, and referring noise to the input, is very similar to that for offsets and drift. As Figure 6 shows, it consists of an ideal noiseless amplifier, a noise-voltage generator in series with either of the inputs, and two uncorrelated noise-current generators, one in parallel with each input. Basic noise-test circuits resemble those for offset voltage and bias current.

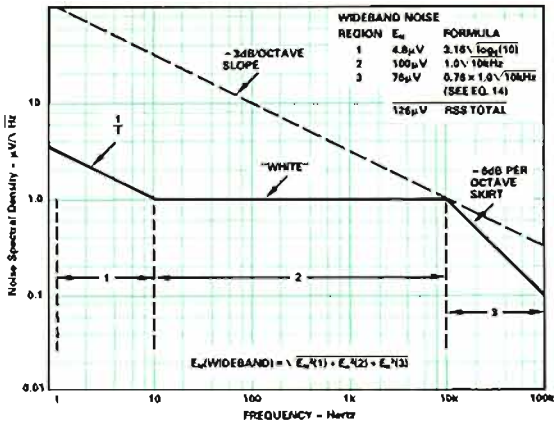


Figure 5. Wideband noise is equal to the root-square sum of components in (1), (2), and (3). For any upper-frequency limit, total noise can be well-approximated by summing just those components in the vicinity of a −3 dB/octave line lowered tangent to the curve. In this example, (1) can be ignored for the wideband case, but not for a cutoff at 20 Hz.

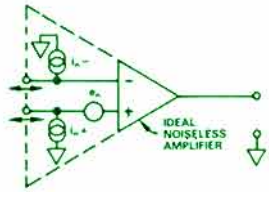


Figure 6. Operational amplifier noise model.

In instrumentation amplifiers, in addition to the input noise sources (especially relevant at high gains), there is also a noise source associated with the output stage; its effect, referred to the input, is seen principally when the amplifier is set for low gains.

Like offsets and drifts, voltage noise is amplified by the "noise gain," (the closed-loop gain of the amplifier with its feedback circuit). Current noise, flowing through impedances, produces noise voltage, just as bias current produces offset voltage.

In addition to the effects lumped within the amplifier, each external resistor's noise contributes to the overall noise total, as though it were in series with a voltage noise generator or in parallel with a current noise generator (the choice depends on which makes the analysis easier). The output noise, in a given bandwidth, depends on the contributions (to the output) of all independent noise sources. Since we assume the amplifier—and all the associated components—to be operating in the linear region, we may calculate the effects separately and combine them by superposition, but in root-square fashion, (they are uncorrelated random signals). In the example of Figure 7, the individual contributions are:

E_A	Amplifier voltage noise	Multiplied by $G = 1 + R_2/R_1$
I_{N-}	Current noise at − input	Multiplied by R_2
I_{N+}	Current noise at + input	Multiplied by $R_c \times G$
E_{Rc}	Voltage noise due to R_c	From eq. (2), multiplied by G
I_{R1}	Current noise due to R_1	From eq. (3), multiplied by R_2
E_{R2}	Voltage noise due to R_2	From eq. (2), direct

When performing root-square summation, it is worthwhile to remember that any noise source less than ¼ of the largest noise source contributes less than 3% to the total and can probably be ignored ($\sqrt{1 + 0.25^2} = 1.03$). Table 1 illustrates a typical calculation for the bandwidth, 100 Hz to 10 kHz, using values previously determined from the 741 curves in Figure 3 (a) and (b), the AD OP-27 curves in (c), and the AD547 voltage noise curve in (d).

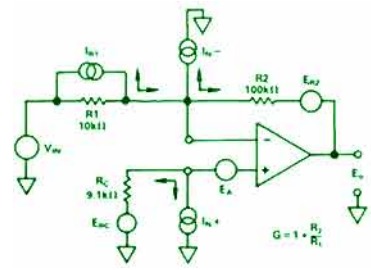


Figure 7. Noise sources in a gain-of-10 op-amp circuit.

Anticipating the reader's question, curves for current noise in FET-input op amps are not often published, because the noise is so low. In junction FETs, current noise is basically equal to the shot noise produced by the leakage current. For the AD547K, the maximum bias current is 25 pA at room temperature. Using (6), $i_n = 0.566\sqrt{0.000025\ \mu A}\ pA/\sqrt{Hz} = 2.8\ fA/\sqrt{Hz}$.

Table 1. Op Amp Noise Calculations in 100 Hz to 10 kHz BW (Δf = 9900 Hz)

Type	Source	RMS Noise	Factor	Output Contribution (μV)
AD741	E_A	1.86 μV	× 11	20
	I_{N-}	54 pA	× 0.1 M	5.5
	I_{N+}	54 pA	× 0.009 M × 11	5.5
	E_{Rc}	1.22 μV	× 11	13.5
	I_{R1}	128 pA	× 0.1 M	12.8
	E_{R2}	4.1 μV	× 1	4.1
	Total	(root sum-of-squares)		29
AD OP-27	E_A	0.3 μV	× 11	3.3
	I_{N-}	40 pA	× 0.1 M	4
	I_{N+}	40 pA	× 0.009 M × 11	4
	E_{Rc}	1.22 μV	× 11	13.5
	I_{R1}	128 pA	× 0.1 M	12.8
	E_{R2}	4.1 μV	× 1	4.1
	Total	(root sum-of-squares)		20
AD547K	E_A	2.3 μV	× 11	25.3
	I_{N-}	0.28 pA	× 0.1 M	0.03
	I_{N+}	0.28 pA	× 0.009 M × 11	0.03
	E_{Rc}	1.22 μV	× 11	13.5
	I_{R1}	128 pA	× 0.1 M	12.8
	I_{R2}	4.1 μV	× 1	4.1
	Total	(root sum-of-squares)		31.6

In this example, it can be readily seen that, with an inverting gain of 10, the effective overall noise—*referred to the input signal*—is dominated by the AD741 and AD547's voltage noise—with significant contributions from the resistors—and amounts to about 3 μV in both cases. On the other hand, with the much quieter AD OP-27, the resistors are the principal source of noise—with about 2 μV, referred to the input signal.

Noise Figure. Even if there were no other sources of noise, the Johnson noise due to the input signal's source resistance would constitute a minimum. The noise contributed by the amplifier circuit, in relation to the noise generated by the source resistance, provides a means of characterizing the noise referred to the signal input. The circuit's *noise figure* is the logarithmic expression of the ratio of the total noise to that contributed by the source resistance. If no additional noise were produced, the total noise would be identical with the source noise and the ratio would be unity, thus the noise figure would be 0 dB. In this particular example, if we were to let the input resistance (R_1) represent the source resistance, the noise figure would become 7.1 (= $20 \log_{10}(29/12.8)$), 3.9, and 7.8 dB for the three cases.

Equivalent noise resistance. The amplifier circuit's noise may be characterized in terms of the Johnson noise, generated by the addi-

tional resistance that would be required to generate an equivalent amount of noise in the presence of an otherwise noise-free circuit; for the above examples, 41, 14, and 51 kilohms.

DYNAMICS

The noise, in the calculations above, is considered to be broadband white noise, with brick-wall filtering and no frequency-shaping elements (e.g., capacitors) in the circuits. Real filters, though, tend to have reduced response near the extremities of the pass band and graduated responses ("skirts") beyond the cutoff frequency; they are likely to pass more noise than a filter having the same cutoff frequency and perfectly sharp cutoff characteristics.

A simple circuit that can introduce us to both real-world considerations is shown in Figure 8. It consists of a resistor, R, considered as a current source, in parallel with a capacitor, C. The noise voltage generated by this circuit will be identical to that obtained using R as a noise voltage generator and a first-order low-pass filter with time constant RC, and cutoff frequency, $1/(2\pi RC)$.

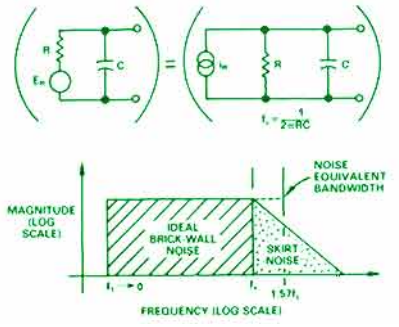


Figure 8. White noise voltage with first-order lag filtering is similar to noise produced by a resistor with a capacitor in parallel and the same RC.

To determine the output voltage in accordance with (9), multiply the resistor's noise current spectral density, i_n, which is flat with frequency, by the magnitude of the impedance of the parallel R-C to determine e_n, then square it, integrate from f_1 to f_2, and take the square-root. Assuming that f_1 is much smaller than f_c, and desiring to determine all the noise within the passband of the filter, we integrate over all f, 0 to ∞. Since the impedance magnitude is

$$|Z| = \frac{R}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}}$$

$$E_n = i_n R \sqrt{\int_{f1}^{f2} \frac{df}{1 + \left(\frac{f}{f_c}\right)^2}}$$

$$E_n = i_n R \sqrt{f_c} \sqrt{\tan^{-1}\left(\frac{f}{f_c}\right)\Big|_0^\infty} \qquad (14)$$

$$E_n = i_n R \sqrt{f_c} \sqrt{\frac{\pi}{2}}$$

$$= 1.25\, i_n R \sqrt{f_c}$$

Thus, the first-order filter's 6-dB-per-octave skirt causes a 25% increase over the noise measured with an ideal sharp-cutoff filter.

We can think of this in two ways. First, the first-order lag filter adds an amount of rms noise equal to $0.76\, e_n \sqrt{f_c}$, i.e., $\sqrt{1.25^2 - 1}$, root-sum-square, to the brick-wall value of $e_n \sqrt{f_c}$. Second, we can think of the filter as being equivalent to a brick-wall filter having an increased bandwidth, or *noise equivalent bandwidth* (N.E.B.) of $(\pi/2)f_c = 1.57\, f_c$. Noise equivalent bandwidth, a useful concept, differs for various filters, depending on order (1st, 2nd, 3rd, etc.), type (high-pass, low-pass, Butterworth, Chebyshef, etc.), and spectral density characteristics of the noise being filtered, e.g., white, pink, shaped.

In similar fashion, overall frequency content of output noise is determined by the shaping effect of the circuit's dynamic elements on the spectral density of the noise from each source. The noise spectral density at the output of the amplifier due to the amplifier's voltage noise (in the absence of current noise) is the product of the closed-loop gain transfer function and the noise spectrum. The output noise produced by noise current in an inverting op amp is determined by multiplying the noise-current spectrum by the impedance spectrum of the feedback element. The overall output noise spectrum is determined by adding the noise spectral densities of output voltage due to all sources, taken independently, at each frequency, in root-square fashion.

This is easier than it sounds, because in practice very little error is incurred by allowing the largest value of noise at any frequency to represent the r.s.s. sum at that frequency. In the few exceptional cases, the largest values can be r.s.s.-added; for this kind of calculation, a calculator that performs vector addition is useful. A graphical technique is helpful in visualization.

ANOTHER EXAMPLE

Consider the example of Figure 9, a dynamic version of one of the examples given previously, employing the 741-type op amp and assuming a feedback capacitance, in parallel with R_2, of 100 pF. The AD741 has a −6 dB/octave rolloff and unity-gain bandwidth of 1 MHz; assume an input capacitance (amplifier and wiring) of 10 pF from the inverting input to common, and that R_c is bypassed by a 0.1 µF capacitor. We wish to determine the overall noise spectral density and the wideband rms noise.

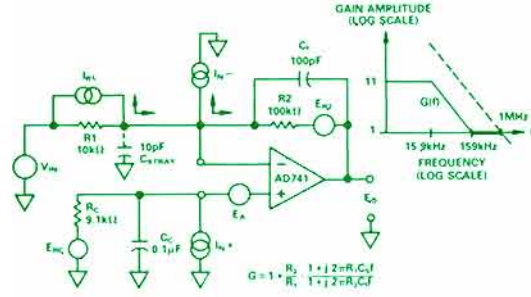


Figure 9. Dynamic version of Figure 7.

Table 2 describes the noise sources, the spectral density of the noise generated by each source, and its gain-bandwidth-output function. For the circuit shown, the noise gain is 11 V/V at dc, breaking at 15.9 kHz, dropping at 6 dB/octave to unity at frequencies above 159 kHz, and rolling off with the amplifier's gain at 1 MHz.

Figure 10 is a plot of the individual contributions of all six sources to the output, plus a plot of the combined noise spectral density, obtained by r.s.s. summation at various critical frequencies (e.g., 1 Hz, 100 Hz, 175 Hz, 300 Hz, 1 kHz, 2 kHz, 16 kHz, 160 kHz). Note that, at low frequencies, the amplifier's voltage and current 1/f noises are the most-significant contributors, while at high frequencies, e_A and R_1 are the most-significant contributors. R_2's contribution is insignificant, and R_c is a minor contributor, principally in the 100-200 Hz range.

Table 2. Calculations for spectral density plots of Figure 10.

Noise Source	Frequency or Band Hz	Generated Spectral Density	Output Spectral Density, $\mu V/\sqrt{Hz}$: 1 Hz	100 Hz (e_A corner)	175 Hz (0.1 μF corner)	2 kHz (I_N corner)	15.9 kHz (C_t corner)	159 kHz (C_c corner)	1 MHz (AD741 corner)
e_A	1	220 nV/√Hz	2.4	0.35	0.29	0.22	0.2	0.02	0.02
	10	71							
	100	32							
	175	26							
	2k +	20							
i_{N-}	1	22 pA/√Hz	2.2	0.23	0.19	0.071	0.055	0.0055	0.0009
	10	7.1							
	100	2.3							
	175	1.8							
	2k	0.71							
	10k +	0.55							
i_{N+}	Same as for i_{N-}		2.2	0.23	0.19	0.006	–	–	–
R_c	Broadband	12.2 nV/√Hz	0.134	0.134	0.134	0.012	–	–	–
R_1	Broadband	1.29 pA/√Hz	0.129	0.129	0.129	0.129	0.129	0.013	0.002
R_2	Broadband	41 nV/√Hz	0.041	0.041	0.041	0.041	0.041	0.004	–

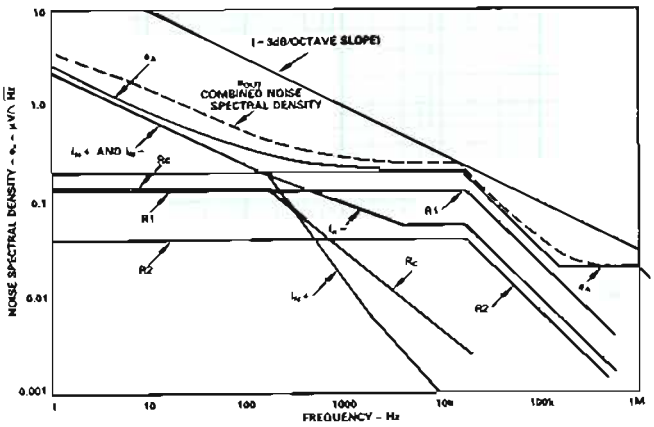


Figure 10. Output voltage contributions of noise sources in the circuit of Figure 9 and combined noise spectral-density.

The rms noise can be approximated in 3 "brick-wall" regions: 1/f, from below 1 Hz to about 400 Hz (extrapolated corner), with K = 3.9 $\mu V/\sqrt{Hz}$, white noise with e_n = 250 $nV/\sqrt{Hz}$, from that point to the 15.9 kHz rolloff, and white noise at 20 $nV/\sqrt{Hz}$, from about 159 kHz to the 1-MHz amplifier rolloff. The contributions and sum, referred to output and signal input, are:

		R.T.O.	R.T.I.
1/f noise (400Hz down to 0.1 Hz): $3.9\sqrt{\ln(4000)}$	=	11 μV rms	1.1 μV rms
Wideband noise (to 15.9 kHz and including the skirt from 15.9 kHz)): $0.25\sqrt{15.9\,kHz} \times 1.25$	=	39 μV rms	3.9 μV rms
Total noise in passband:		41 μV rms	4.1 μV rms
H-Four-of-band noise from 159 kHz to 1 MHz and including the NEB of the 1-MHz skirt: $0.02\sqrt{(1.57 \times 1 - 0.159)MHz}$	=	24 μV rms	2.4 μV rms
Total rms noise:		48 μV rms	4.8 μV rms

NOISE TESTING

In order for users to predict that an amplifier will be sufficiently quiet for a given application, with a guarantee that goes beyond the "typical" curves given in the data sheet, the manufacturer must guarantee a set of maximum noise specifications. Here is an example, the specifications of noise for the AD OP-07:

Band	Typical	Maximum	Units	Remarks
0.1 Hz–10 Hz	0.35	0.6	μV p-p	Voltage noise
f_o = 10 Hz	10.3	18.0	$nV/\sqrt{Hz}$	V spectral density
f_o = 100 Hz	10.0	13.0	$nV/\sqrt{Hz}$	V spectral density
f_o = 1 kHz	9.6	11.0	$nV/\sqrt{Hz}$	V spectral density
0.1 Hz–10 Hz	14	30	pA p-p	Current noise
f_o = 10 Hz	0.32	0.80	$pA/\sqrt{Hz}$	I spectral density
f_o = 100 Hz	0.14	0.23	$pA/\sqrt{Hz}$	I spectral density
f_o = 1 kHz	0.12	0.17	$pA/\sqrt{Hz}$	I spectral density

Noise is usually specified in this way, peak-to-peak at low frequency and either spectral density or band-limited rms noise at higher frequencies. The manufacturer further specifies whether these specs have been 100% tested in production or on a sampling basis. Whether the noise is tested in characterization, in production, or by the user to verify noise performance of an incoming lot of devices, the test definition and circuitry should be standardized.

Figure 11 shows a typical test scheme, and the measurement circuitry employed. The device under test (DUT) is connected for a noise gain of (say) 10. A pair of 1-megohm resistors in series with the input terminals permit current noise to be measured, and a pair of shorting switches permit voltage noise and the current noise at either input to be measured individually. The output of the DUT is applied to a bandpass filter with a further gain of 10; the high-pass makes the noise measurement independent of the DUT's dc offset. The low-pass filter is a two-pole Butterworth. With the high-pass, the filter is programmable for 7 different frequency bands. Measurements are performed by either the rms-to-dc converter or the system voltmeter (for discrete sampling).

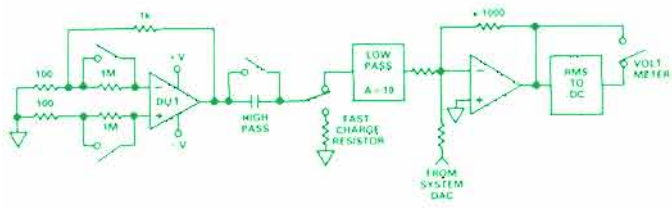


Figure 11. Noise-test circuit for op amps.

The bandpass filter has a noise effective bandwidth (N.E.B.) comparable to the band in question, e.g., 10 to 1000 Hz. The test system must take into account the DUT's reduction of bandwidth with increased gain, if it is a factor in the measurement. A wideband true-rms voltmeter measures the output of the filter and either interprets it directly as rms noise in the band, or calculates noise spectral density. At lower frequencies, the output is sampled, and calculations are performed to determine the rms, the peak-to-peak amplitude, and the presence of popcorn noise.

Both white noise and 1/f noise are random and have benign statistics. However, popcorn noise with sufficient amplitude to be readily detectable is of concern because it is an indicator of defective processing. Also, its "burst" nature (over periods from microseconds to seconds) is particularly annoying in many applications. When looked at with an oscilloscope, it is readily visible as a shift between levels (Figure 2c). How does a *computer* determine within a short time if substantial popcorn noise is present?

In one easy-to-automate approach, the criterion used to identify popcorn noise is: for successively sampled values of the output of the DUT and filter, are there any differences (jumps) that exceed 4 × rms (4 σ)? If so, these jumps, which have a probability of less than 0.01%, are taken to be "hits" of popcorn-noise (Figure 12).

NOISE TESTING WITH THE LTS-2000 FAMILY

The LTS-2000 family of device testers are powerful low-cost computer-based self-contained benchtop test systems that can test a wide gamut of linear, digital, active, and passive devices, including amplifiers, d/a and a/d converters, digital logic ICs, discrete semiconductors, and passive components. Calibration is automatic and tests are performed quickly and automatically in accordance with either menu-driven or BASIC-programmed software pro-

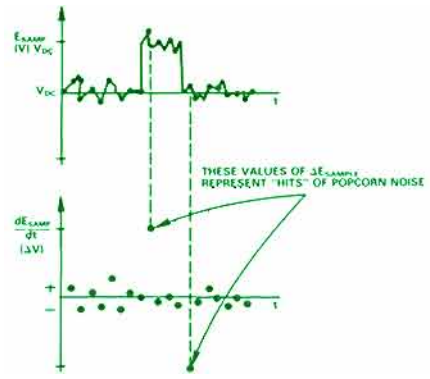


Figure 12. Examining the sampled signal for popcorn noise by differencing.

grams. Documentation is available as pass/fail, quantitative, and statistical information.

Flexible hardware, as well as software, programs the system for testing specific devices. Plug-in family boards provide the rapid-change circuitry essential to testing such families as DACs, ADCs, amplifiers, etc. Circuitry for performing general- or special-purpose tests (such as noise) is wired to a device-test socket assembly, which plugs into the family board. Devices under test are plugged into test-socket cards, which are wired for specific devices and plugged into the socket assembly.

The LTS-0613 Noise-Test Socket Assembly (soon to be announced*), in conjunction with the op-amp family board, enables users of the LTS-2000 family to perform noise testing on op amps—a capability available for the first time in benchtop ATE.

When used in conjunction with the LTS-2100 Op-Amp Family Board, the LTS-0613 tests noise, as well as the full range of parameter tests that the LTS-0600 Op-Amp Socket Assembly has been providing, for single, dual, and quad packages. It permits measurement of noise spectral density and peak-to-peak values for both voltage and current noise over a range of seven different bandwidths; the associated software also provides a routine for detecting popcorn noise.

The LTS-0613's circuit is quite similar to the block diagram of Figure 12, and—in fact—performance of the tests is similar to the technique described above. Automatic switching is available to choose among the four op amps in a quad. The high-pass filter, which serves the function of blocking any DUT offsets, can be initially switched—prior to testing—to have low values of resistance so that the blocking capacitor can be rapidly charged; without it, the wait for the circuit to settle before performing tests at the low end (0.1 to 10 Hz) would greatly reduce the speed of testing.

The DUT is wired for a gain of 10, a compromise that allows its noise to be amplified to a level significantly higher than that of the filter and gain stages, while retaining as large a bandwidth as possible for measurement of noise in the higher-frequency bands. Gain is also taken in the filter, which employs low-noise amplifiers, and in a pair of post-filter amplifiers. The overall gain from the DUT input is 100,000 V/V.

Relay-switchable filter time constants permit tests over the following bands: 0.1 to 10 Hz; 0.1 to 100 Hz; 1 to 100 Hz; 1 Hz to 1 kHz; 10 Hz to 1 kHz; 10 Hz to 10 kHz; and 100 Hz to 10 kHz. Output to the system is software-switchable between an analog true-rms circuit, for wideband measurements, and individual samples, for the low frequencies. Sampling permits both accurate low-frequency rms computations and examination for popcorn hits.

The software is set up as a subroutine to be called from the user's BASIC test program. All variables (such as test limits, bandwidths, choice of voltage noise, current noise, or both) are listed in documentation that accompanies the socket assembly. The user simply establishes the appropriate variables in the test program and then calls the subroutine. The flow chart in Figure 13 is a diagram of the subroutine's procedure.

When the testing has been completed, the system prints the results in a form similar to the datalog shown in Figure 14, which depicts the test results (vs. limits) of 16 critical parameters for an AD OP-07E.

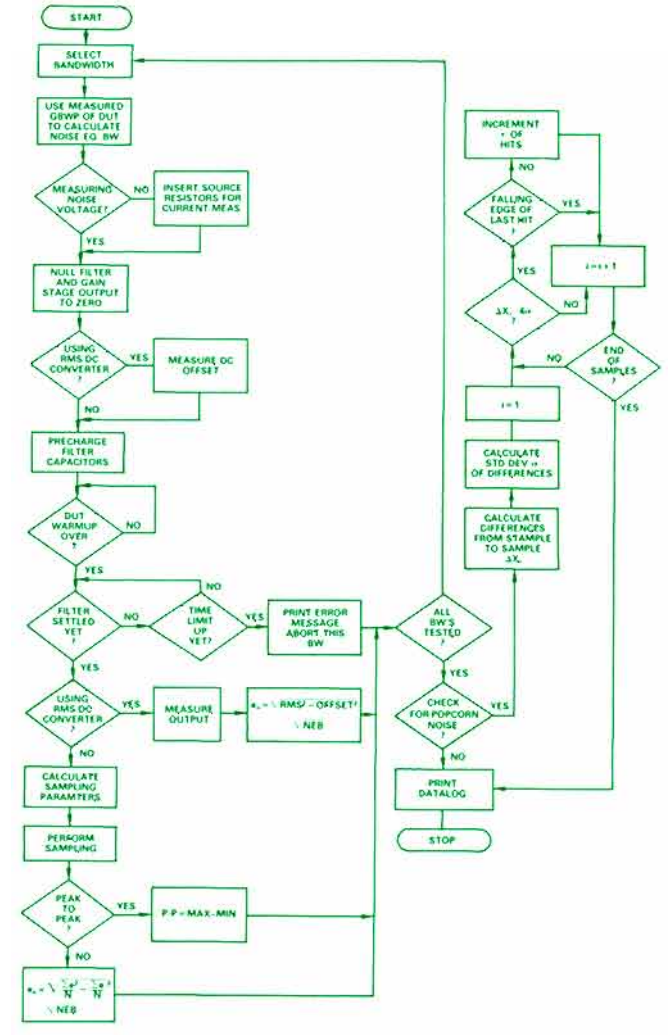


Figure 13. The LTS-0613 noise-test subroutine.

```
DEVICE 2 TESTING
T# 1        3.13 MA      +I SUPPLY                 [ 0.1 TO 4 MA ]
T# 2       -3.13 MA      -I SUPPLY                 [ -4 TO -0.1 MA ]
T# 3       33.38 UV      VOS 50 OHMS               [ -75 TO 75 UV ]
T# 4        -2.4 NA      +I BIAS                   [ -4 TO 4 NA ]
T# 5        -3.0 NA      -I BIAS                   [ -4 TO 4 NA ]
T# 6          .7 NA      I OFFSET                  [ -3.8 TO 3.8 NA ]
T# 7      7654.8 K       AOL                       [ 300 TO 1E12 K ]
T# 8       140.0 DB      CMRR                      [ 106 TO 1E12 DB ]
T# 9         3.2 UV/V    PSRR                      [ -20 TO 20 UV/V ]
T# 10       14.01 V      +V OUT                    [ 10.5 TO 15 V ]
T# 11     -13.62 V       -V OUT                    [ -15 TO -10.5 V ]
T# 12       9.15 NV/RH   NOISE VOLT (100-10K HZ)   [ 0 TO 13 NV/RH ]
T# 13       9.47 NV/RH   NOISE VOLT (10-1K HZ)     [ 0 TO 18 NV/RH ]
T# 14        .23 PA/RH   NOISE CUR (10-1K HZ)      [ 0 TO 0.8 PA/RH ]
T# 15      13.86 PA      P-P NOISE ] (.1-10 HZ)    [ 0 TO 30 PA ]
T# 16          0 HITS    POPCORN NOISE             [ 0 TO 0 HITS ]
PASS BIN 1
```

Figure 14. Data-log of test results on OP-07E, employing the LTS-0613. Columns are test number, actual measurement, description, and pass limits.

*For technical data, use the reply card.

SECOND-GENERATION MONOLITHIC RMS-TO-DC CONVERTER

AD637 Combines High Accuracy, Wide Bandwidth, and Versatility

Twice the Bandwidth and Less than Half the Nonlinearity of the AD536A

by Lew Counts and Charles Kitchin

In 1977, the industry's first monolithic rms-to-dc converter, the Analog Devices AD536, was introduced in this Journal (11-2). It was one of the earliest IC products to have its performance enhanced by laser trimming at the wafer level. Since then, an improved version, the AD536A, and a low-level version, the AD636 (both based on the same design) have been introduced. In these pages, we introduce a second-generation descendant of the AD536, a device with greatly improved accuracy and much higher bandwidth at low levels as well as some interesting features that permit it to be used as a multifunction component.

The AD637* is a monolithic rms-to-dc converter in a 14-pin DIP. It accepts waveforms of any shape, including dc, and produces an output which is proportional to the input's rms value. Its improved performance includes both high accuracy at all input levels, with nonlinearity less than 0.02% of full scale over its entire 0 to 7-volt input range, and wide bandwidths—up to 8 MHz for 2-volt-rms input signals. A logarithmic output is also available for applications that require a decibel interpretation of the output signal.

Figure 1 is a plot of worst-case error vs. rms voltage level for input levels from 0 to 8 V rms. Besides showing how low the errors can be with no external trim of the AD637, it also illustrates the extent of optional accuracies available following the introduction of the AD637, from the lowest-error AD637K to the lowest-cost AD536AJH. Errors can be reduced even further by external trimming of the AD637's scale factor and offset.

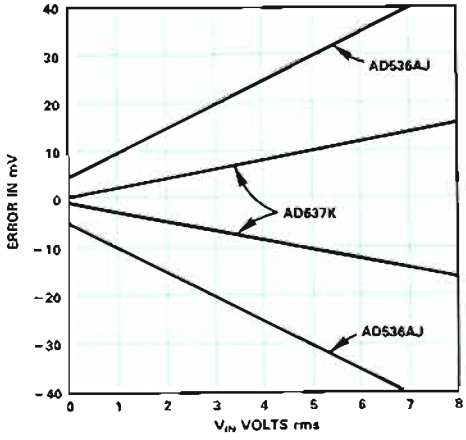


Figure 1. Error of rms devices as a function of rms amplitude.

Figure 2 shows frequency responses typical of the AD637 (dashes) compared with those of the AD536A (solid) at various rms input levels. It should be apparent that the AD637's bandwidth is about twice that of the AD536A at all levels and is greater than 100 kHz at low levels (e.g., 10 mV rms).

In addition to performance improvements, the denominator feedback—which was connected internally in the AD536A—has been

*For technical data, use the reply card.

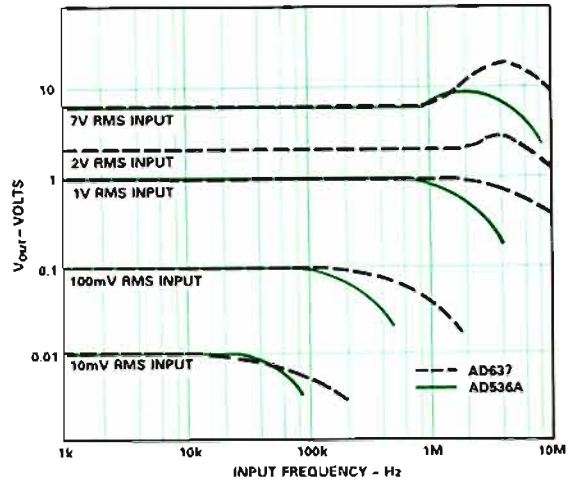


Figure 2. Bandwidth of the AD637 compared with the AD536A.

"unbundled" in the AD637 for greater versatility and increased design freedom in applications. The AD637 can be readily connected to compute:

- The square and mean-square of the input signal
- The vector sum or the sum of the squares of two or more independent time-varying voltages using two or more AD637s connected together.
- The root-mean-square of very slowly varying (less than 1 Hz) input signals.

A BRIEF REVIEW OF RMS

RMS, or root mean-square, is a fundamental way of summarizing and measuring an ac signal's magnitude. It has meanings that are relevant from both the mathematical and the practical physical point of view.

In the physical sense, the rms voltage or current value assigned to an ac signal is the same as the dc voltage or current that would be required to generate an equivalent amount of heat in the same resistive load. For example, an ac signal of 1 volt rms—irrespective of waveshape—will produce the same amount of heat in a resistor as a 1-volt dc signal. It doesn't matter whether the ac voltage is a pure sine wave with a peak amplitude of $\sqrt{2}$ volts, a symmetrical square wave of ± 1-volt amplitude, or a zero-average noise voltage with undefinable peak amplitude. The rms voltage is defined as

$$V_{RMS} = \sqrt{\text{average}(V^2)} \qquad (1)$$

where V is the set of all consecutive discernible "instantaneous" values of voltage in the averaging interval.

The rms value of an ac-coupled waveform is of especial value when random noise and vibrations are measured. The reason is that the rms value of a waveform is identical to the standard deviation of that signal. The relationship is independent of signal type; for

noise, rms equals the standard deviation, whether the noise is gaussian or has some other type of distribution.

For an analog device that computes rms, the bandwidth must be sufficient to deal with the input signal's "instantaneous" values; in addition, the averaging time must be sufficiently long to allow adequate filtering at the lowest frequencies of operation desired. Since the averaging time-constant in effect sets the time during which the device "holds" the input signal during computation, its value directly affects the low-frequency accuracy of an rms measurement.

A WORD ON RMS CONVERTER DESIGN

There are two popular approaches to designing analog true-rms circuits, thermal and computational. The most typical *thermal* approach is to allow the input signal to heat a resistor, then cause a feedback loop to adjust the temperature of a similar resistor by sensing the temperature difference while continuously adjusting the dc voltage across the second resistor to keep the temperatures equal; at equilibrium, the dc voltage across the second resistor is equal to the rms voltage across the first resistor. While this approach can result in very accurate, wideband designs, the resulting circuitry tends to be both expensive and power-hungry.

Computational rms-to-dc converters perform rms computations directly by squaring the input signal, averaging it, and computing the square root. This can, of course, be done digitally, either on-line or off-line. However, digital computation of rms requires considerable commitment of equipment, software, and computing time, especially if the rms is required continuously in real time for wideband signals. On the other hand, the rms can be computed in real time while the signal is in analog form, with predictable accuracy, using a single monolithic chip and minimal external circuitry.

It is tempting to consider explicit computation, in which circuits that perform the squaring, averaging, and rooting operations are cascaded in sequence. But this is not the best method, because the squaring operation doubles the number of decibels of dynamic range during the computation; for example, if the signal range is from 2 volts to 100 millivolts (26 dB), the voltage after the squaring circuit would range from 4 volts to 10 millivolts (52 dB). For this reason, the AD637, like most modern rms converters, uses an implicit computational approach combining logarithmic computation and feedback circuitry; signals with extra-wide dynamic range do not appear explicitly in the computation. The result is an rms device with about 60 dB of dynamic range (7V rms to 7 mV rms).

Figure 3 demonstrates the principle employed in the AD637 and other rms devices manufactured by Analog Devices. First, the signal is accurately full-wave rectified (without filtering) in the absolute-value section. Next, the device computes the logarithm of the resulting absolute-value signal and doubles it, producing, in effect, the square of the input signal (i.e., $2 \log X = \log (X^2)$); from it, the log of the output signal is then subtracted, performing a division (i.e., $\log (X^2) - \log Y = \log (X^2/Y)$). The inverse of the logarithm (i.e., X^2/Y) is computed by an exponential operation; and the result, after averaging by a low-pass filter, becomes the output signal (i.e., Y = average (X^2/Y)). The output is fed back; its logarithm is computed and fed to the subtraction stage, resulting in division by the output. If X is equal to V_{in} and Y is equal to V_{out} then, since the loop enforces the condition,

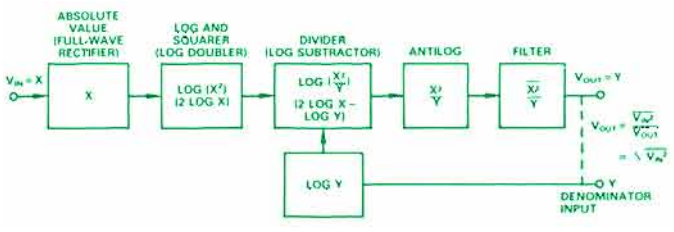


Figure 3. Implicit logarithmic rms computation.

$$V_{out} = \text{average}\left(\frac{V_{in}^2}{V_{out}}\right) \quad (2)$$

and assuming that V_{out} is essentially constant in relation to $(V_{in})^2$ due to adequate low-pass filtering:

$$V_{out} = \sqrt{\text{average}(V_{in})^2} \quad (3)$$

Thus, the relationship is enforced by feedback; division by the output results in the computation of the square root.

In the actual implementation, voltages are converted to currents, with all of the logarithmic operations taking place in a tightly knit central core (more like that depicted in Figure 4, rather than in the neatly delineated separate sections of Figure 3). While the AD637's core is similar to that of the AD536 (*Dialogue* 11-2), a much-improved crest-factor compensation scheme is employed to permit operation at significantly higher current densities while achieving smaller errors than those of the AD536A. An 11% duty cycle (or crest factor of 3) adds only 0.1% to the sine-wave error, and for a crest factor of 10 (1% duty cycle), the error is increased by only 1%. The reduced crest-factor error is of particular importance when complex waveforms, such as those occurring in switching-type power supplies, are being processed.

FEATURES OF THE AD637

Figure 4 is a combined block diagram and connection diagram of the AD637. The signal, via pin 13, is seen going through the absolute-value, squarer/divider, and current-to-voltage output-amplifier stages, finally arriving at the output (pin 9). The filter amplifier (key to the improved linearity) converts the core's output current to a buffered output voltage which can drive load currents of up to 5 mA directly. An external capacitor, C_{AV}, is connected across the amplifier's 25 kΩ (nominal) internal feedback resistor, R_F. The averaging time constant, $C_{AV} R_F$, is independent of signal level, an improvement over the AD536A. In the standard rms connection, the feedback path is completed via the denominator input voltage-to-current converter at pin 6.

Apart from the basic rms-to-dc function, there are several other features of interest. Although the device is laser-trimmed on the wafer to an offset of less than 0.5 mV, it has a provision for external offset trim for user fine-tuning. A chip-select terminal (pin 5) provides for powering down the chip, reducing the power-supply drain from 3 mA max (about twice that of the AD536A) to 450 μA max when invoked; it is a useful feature for energy conservation in battery operation and for multiplexing a number of measurement channels performing rms-to-dc conversion.

Another useful feature is the internal buffer, an uncommitted unity-gain non-inverting amplifier, accessible via pins 1 and 14. It is helpful in various ways—for example, providing additional filtering or buffering the dB output (pin 7).

Device bandwidth has been raised by increasing the signal current in the absolute-value stage and by the use of a high-speed process in manufacture; the result is a useful bandwidth of up to 8 MHz

(at 2-V rms input)—a substantial improvement over the AD536A, as Figure 2 shows.

APPLICATIONS

Standard RMS Connection. Only one external component, C_{AV}, is needed for complete high-accuracy rms computing (Figure 4).

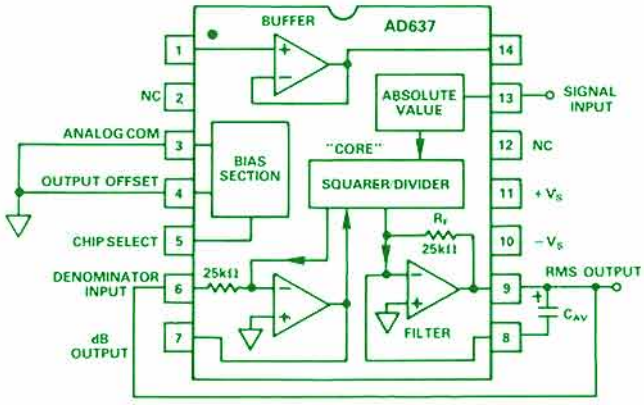


Figure 4. Block diagram and pin connections of the AD637.

The maximum error for input voltages from 0 to 7 V rms will be 0.5 mV ± 0.2% of reading, at mid-band audio frequencies. The internal buffer amplifier, not used here, is freed for other tasks. For a range of low frequencies, the finite averaging time of the converter will produce an additional error, principally ripple, varying inversely with signal frequency and averaging time-constant:

$$\%\ \text{peak ripple} = \frac{50}{\sqrt{1 + 40\tau^2 f^2}} \qquad (4)$$

in % of the rms level; $\tau = R_1 C_{AV}$ and f is signal frequency in hertz.

If C_{AV} = 1 μF, peak ripple with a 380-Hz sine wave will be about 1% of reading. The error will be reduced in proportion to increased C_{AV}, but response time to signal amplitude changes increases proportionally. A better solution is to reduce the ripple by following the AD637 with a low-pass filter; suitable filters (which can use the on-chip buffer) are described on the AD637 data sheet.[1]

The AD637 will compute the root sum-of-squares of an ac input signal that has a dc component. To measure the ac component only, the signal may be coupled to the AD637 by insertion of a capacitor in series with the input terminal. A 1-μF capacitor will produce a −3-dB frequency of about 20 Hz; for lower frequencies, use tantalum capacitors with 20-V ratings connected back-to-back in series.

μP-Controlled Averaging/Settling Time-Constant. Figure 5 shows one example of the benefits realizable from a denominator input that can be connected externally. In this circuit, a digitally controllable switch permits a choice among 4 averaging/settling time constants.

For low frequencies, such as 10 Hz, an external filter with a 1-second time constant—for settling to within 1% of final value in 4.6 seconds—should have a sufficiently long time constant for low error. However, at higher frequencies, e.g., 10 kHz—or for inputs which have most of their energy at higher frequencies—it would be useful to switch the time constant quickly and automatically to a much smaller value, such as 1 ms, with settling time of 4.6 ms.

[1] A more-thorough discussion of averaging errors—and a wealth of additional useful information—can be found in the 56-page *RMS-to-DC Application Guide*, available *free* upon request (see page 30).

This would permit readings in that frequency range with a minimum of delay.

In the circuit of Figure 5, one of 4 time constants—1 ms, 10 ms, 100 ms, and 1 s—is established by switching an appropriate resistor between the AD637's output and a 1-μF filtering capacitor, to form an external single-pole filter buffered by the on-chip follower, *inside the AD637's feedback loop.*

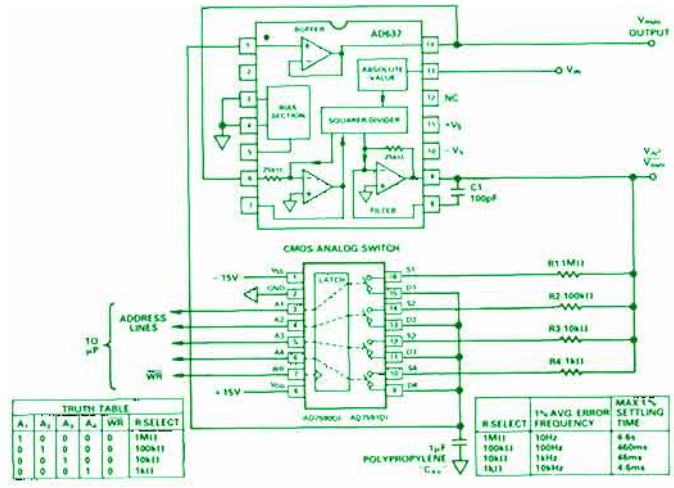


Figure 5. RMS converter with digitally controlled averaging/settling time, independent of signal amplitude.

The time constant, controlled by digital logic, can be switched by a microprocessor. The μP must have a means of determining the frequency content of the signal, and it must be programmed to decide which time constant to use.

The values shown here, and the 10:1 relationships between them, were chosen just as an example. Different values of time constants, and different incremental relationships between them (for example, linear or logarithmic) may be selected to fit your application. The upper limit on resistance is established by the 1-nA bias current of the AD637's internal buffer follower; in this example, resistance was limited to 1 megohm to keep the offset below 1 mV. For longer time constants, use more capacitance; for shorter time constants use less resistance.

One caution: this circuit may saturate (without damage) on transient spikes as a consequence of the very low value of feedback capacitance (C_1 = 100 pF) around the internal amplifier. In this case, the effective C_{AV} is the capacitor in the filter; the 100-pF capacitor is there solely for stability. Since C_1 entails minimal filtering, the output voltage, at pin 9, responds to the *instantaneous square* of the input rather than the *mean square*. The resulting higher crest factors can be handled by increasing C_1 by a factor of 100 or more, as long as the feedback circuit's time constant is kept substantially less than that of the switched time constants to minimize additional time delays.

There are many other possible applications that can profitably use the fast, precise, versatile AD637, for example, controlled squaring and mean-square measurements. While the above example shows μP-controlled switching of filter time constants, the clever designer may wish to consider auto-adaptive possibilities employing all-analog circuitry. With the accessible denominator input, the internal voltage buffer, the log output, and the power-down feature, many exciting new configurations—as yet unknown—await the creative designer's imagination.

FAST, SIMPLE APPROXIMATION OF FUNCTIONS

Use A Lookup Table And a Digital Multiplier To Implement Newton-Raphson Approximations

by Matt Johnson

Now that low-cost, low-power digital multipliers and multiplier/accumulators are readily available (for example, ADI's ADSP-1000 device-family*) it has become possible to implement many digital signal-processing (DSP) applications with high speed. The most common applications are in performing fast Fourier transforms (FFT) or filtering incoming data from either a real-time source or from stored data off-line. However, their utility is not limited to such conventional applications. DSP components can be used, along with applied mathematical convergence theory, to embody algorithms for evaluating scientific functions at high speed.

When exact solutions are not required, approximation techniques—employing parallel computation using hard-wired components—allow us to bypass the long calculation times normally required by CPUs in evaluating scientific functions. Depending on the specific function and the accuracy of the desired solution, the execution time required by a CPU to effect solutions—using its built-in algorithms—can be bettered by as much as two orders of magnitude. For example, a 16-bit 8086 divide takes some 30 microseconds, compared to about 300 ns for the implementation to be described here, using an 8-bit lookup table and a hardware multiplier. Such increased performance can mean the difference between a successful design and a merely interesting one that never gets off the ground.

As an example of the technique, we show how one might implement an approximation of a common function occurring frequently in signal processing systems, the reciprocal ($y = 1/x$). A fast reciprocal is just one multiplication away from a full-blown fast divider, but redundant architectures do exist for implementing the complete division without the extra multiply cycle. We will examine both the theoretical implications and hardware realizations of the technique.

NEWTON-RAPHSON

We will apply the Newton-Raphson recursion algorithm, which is well known to users of mathematical approximation techniques. It is a very powerful algorithm because it produces quadratic convergence (i.e., each iteration provides a doubling of precision). To begin, a guess is made as to the root of the function (solution for an unknown value) in the vicinity of the desired root. The derivative (slope) of the function is evaluated at the guessed value, leading in turn to new, successively closer iterations (Figure 1). The method may be applied to approximate any "well-behaved" function, i.e., a function not exhibiting zero derivatives within the region where the function is expected to converge.

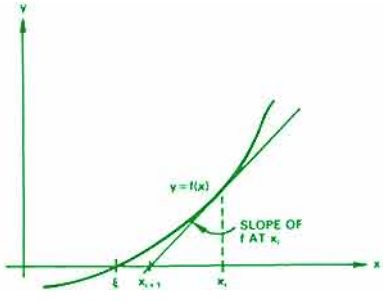


Figure 1. Well-behaved convergence using Newton-Raphson. The first guess is x_i, the second is x_{i+1}.

The significance of "well-behaved" is apparent in the following cases. Figure 1 traces the algorithm as it converges through two iterations towards a root, ξ, of a monotonic function. As the plot shows, the guess for the *i*th iteration was x_i; the slope is determined at x_i, and the point where it intersects the x-axis is the new guess, x_{i+1}. Notice how successive solutions converge quickly. Figure 2, on the other hand, illustrates two examples in which a naughty function (having zero derivatives) prevents convergence. Fortunately, the *reciprocal* is well-behaved for all values of $x \neq 0$.

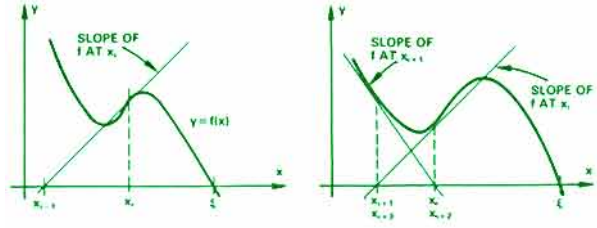


Figure 2. No convergence with zero-derivative functions.

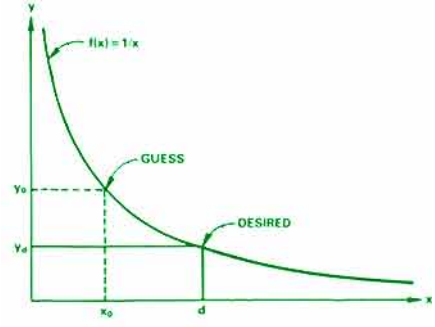


Figure 3. Functional relationship, f(x) = 1/x.

The Newton-Raphson recursion is derived using a first-order Taylor series expansion in the following manner (figure 3). Assume we wish to find the reciprocal of a value of x we will call d (thus, $y_d = 1/d$), knowing only the functional dependence, $f(x) = 1/x$, and the value of y at an arbitrary point, x_0: $f(x_0) = y_0$. We define an error function, $F(y) = 1/y - d$, whose root occurs at $F(y_d)$, i.e.,

$$F(y_d) = 1/y_d - d \quad (= 0) \tag{1}$$

When it is solved for y, we will have the desired value of the reciprocal at d, y_d.

We write a first-order Taylor series expansion of this error function about the point, y_d, giving us a linear approximation to the desired solution. Hence we have, for the *n*th iteration, y_n,

*Use the reply card for technical data.

$$F(y_d) \simeq F(y_n) + (y_d - y_n)F'(y_n) \quad (2)$$

Equating this expansion to zero (to minimize the error) and generalizing y_d as y_{n+1} (the improved guess), equation 2 becomes:

$$0 = F(y_n) + (y_{n+1} - y_n)F'(y_n) \quad (3)$$

Solving (3) for the value of y_{n+1} (which we are seeking),

$$y_{n+1} = y_n - F(y_n)/F'(y_n) \quad (4)$$

This is the general form of the Newton-Raphson recursion. For the specific case of the reciprocal, we substitute the error function (from equation (1)) and its derivative ($F'(y_n) = -1/(y_n)^2$):

$$y_{n+1} = y_n + y_n^2(1/y_n - d)$$
$$= y_n(2 - d * y_n) \quad (5)$$

PREPARATIONS

How do we make our first guess, y_0, to start the Newton-Raphson iteration? The most effective way is to address a lookup table (ROM), having a relatively small number of fixed points, with a nearby value of x. Although the hardware could be simplified (eliminating ROM and associated circuitry) by always starting at a fixed arbitrary value, we would find that it is a somewhat inefficient approach, because the resulting higher initial error leads to more iterations than we want (albeit still faster than an exact solution executed by a CPU).

When lookup tables and finite-precision hardware are used, an important aspect of approximation techniques is data normalization. We would like to match the full operating range of a device to the full range of the function. In the interest of restricting the range of the function's argument to fully utilize the limited precision of hardware multipliers (or conversely, to maximize the dynamic range of the result), it is common practice to shift the argument (viz., successively multiply or divide by 2) until it is in the range within which a sufficiently correct answer can be obtained most efficiently. After the approximation technique has been applied, the result is denormalized (i.e., restored to its appropriate range).

Restricting discussion to positive values (a rather trivial stipulation), the range of the reciprocal is from 0 to +infinity. When using a lookup approach for generating the first guess: for a given table size, the smaller we limit the range of the argument, the closer the first guess will be. In the case of the reciprocal, we normalize the data to the range ½ to 1^- (the superscript used in 1^- denotes all numbers less than but not including 1)*, i.e., data greater than or equal to 1 is right-shifted, and data less than ½ is left-shifted, until the most significant bit appears at the 2^{-1} position. For example, 101.11010 would be shifted right until it became 0.1011101, and 0.0001111 would be shifted left until it became 0.1111000. The resulting truncated reciprocal function is the curve sector shown in figure 4.

To provide a uniformly accurate first guess for the Newton-Raphson recursion, we divide up the normalized dividend range, x, into a convenient number of intervals and assign the midpoint of each interval as our guess for 1/d for all values of d falling within that interval. Effectively, the first guess, $y_0(s)$, becomes a stepwise

*In fractional binary, this range would be 0.1000...0 to 0.1111...1.

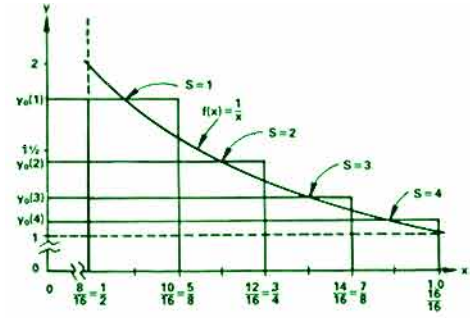


Figure 4. Normalized reciprocal 1/x and stepwise approximation $y_0(s)$ with j = 2.

approximation to f(x) = 1/x, being constant in each of 2^j equal segments between ½ and 1^-. The true reciprocal at the midpoint of each segment, s(x), may be calculated using (6).

$$y_0(s) = \frac{2^{j+2}}{2^{j+1} + 2s - 1} \quad (6)$$

Such a scheme is seen in Figure 4; the number of segments has been limited to 4 (j = 2) for illustrative purposes. For example, if s = 3, the value of $y_0(3) = 16/(8+6-1) = 16/13$. This is the exact reciprocal of 13/16, the midpoint between 3/4 and 7/8.

It will prove useful to make a few observations about the normalized argument. Consider, for instance, the format of 16-bit binary numbers ranging from ½ to 1^-:

$$d = 0.1\,i\,i\,i\,i\,i\,i\,i\,i\,j\,j\,j\,j\,j\,j\,j \quad (7)$$

In (7), d is referred to as having a "1.15" format (one bit to the left of the decimal, and 15 to the right). This useful convention makes it easy to locate the proper decimal position of the product formed by two arbitrarily formatted numbers. We simply add the number of bits to the left and to the right of both operands, giving us the correct format of the resulting product. For example, 1.01 × 1.001 = 01.01101; we can predict the format of the product, 2.5, from the 1.2, 1.3 formats of the operands. If either operand is less than 1.0, the leftmost bit of the product will always be 0.

By virtue of the normalization, we know that the integer portion is 0 and the MSB of the fractional portion of the number will always be 1 (i.e., 2^{-1}); the rest of the number (2^{-2} and on...) remains arbitrary. The trick is to use the most significant part of the arbitrary portion of the number (say, the first eight bits: 2^{-2} through 2^{-9}, or iiiiiiii) as an address into a lookup table whose contents are simply the reciprocal of the address (eq. 6).

Since ½ to 1^- is the range of the normalized d, its actual reciprocal lies in the range, 2 to 1^+, and we must reserve the 2^1 bit position for the result. But, because the approximation is computed to be the *midpoint* of each interval, the table contents will only have a range of 2^- to 1^+; i.e., the 2^1 bit is not needed in the table. Furthermore, since we know that the lookup value will always have the 2^0 bit = 1, we need only store the fractional portion of the guess in the table, manually setting the 2^0 bit at the input to the multiplier. Thus, we obtain a 9-bit initial guess with only an 8-bit lookup.

IMPLEMENTATION

Figure 5 is a block diagram of a setup to compute the result of equation (5). The procedure is to compute $d*y_n$, subtract it from 2, then perform the second multiplication (by y_n). For speed and

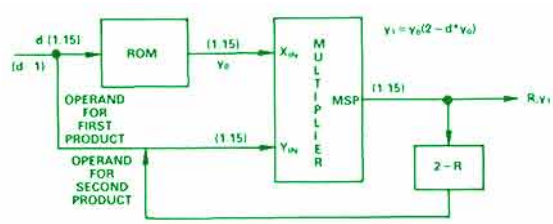


Figure 5. Multiplier layout for reciprocal calculation.

simplicity, the multiplications are 16-bit multiplications, in which only the 16-bit most-significant product (MSP) is used.

The first term formed is the $d * y_0$ term; its upper byte (most significant product—MSP—from the multiplier) is a 16-bit number in the 2.14 format. A single bit arithmetic left-shift (utilizing the format-adjust output option of the multiplier, FA = 0), dropping the leading 0 (we know that the first digit is 0, because the first digit of d is 0), is used to reformat the result back to the 1.15 format in preparation for the second multiply of the iteration, y_0 $(2 - d * y_0)$. Following (5), the shifted result is subtracted from 2 (in the appropriate format) and written back into the multiplier over the former Y register contents of d in preparation to take the product of y_0 and the bracketed expression. The second multiply completes the first recursion; the result may be read directly in the 2.14 format, or shifted (again using FA = 0) and read in the normalized 1.15 format if desired.

ERRORS

Besides the error of fitting the function with a limited number of recursions (which turns out to be negligible after only a single trial), there are also errors of computation. The two principal sources of computational errors are the limited ROM resolution (only 256 trial points) and the multiplication scheme.

The error analysis of this hardware reciprocal scheme is fairly straightforward. For the product, $y_0 * d$, we know that y_0 is in error by an amount less than 2^{-8} (since we assumed an 8-bit lookup table); call this error e_0. That is, $y_0 = 1/d + e_0$. Due to feeding back only a single-precision intermediate result (i.e., the MSP of the multiplier, left-shifted by 1 bit) as an operand to the second multiply, we introduce a known computational error, e', such that $y_1 = y_0[(2 - d * y_0) + e']$.

We may now substitute the error terms into eq. 5 for the first recursion (y_1 ideally $= y_0[2 - d * y_0]$):

$$y_1 = (1/d + e_0)]2 - d * (1/d + e_0) + e'] \quad (8)$$

$$= 1/d + e'/d - (e_0)^2 d + e_0 e' \quad (9)$$

We can combine the three right-hand terms as a single additive error term, e_1,

$$y_1 = 1/d + e_1 \quad (10)$$

Thus, the worst-case error associated with the first iteration may be expressed as:

$$|e_1| = |+e'/d - (e_0)^2 d + e_0 e'| \quad (11)$$

$$\leq |e'/d| + (e_0)^2 |d| + |e_0||e'| \quad (12)$$

This approach may be generalized to describe the error associated with any iteration as:

$$y_n = 1/d + e_n \quad (13)$$

$$y_{n+1} = 1/d + e_{n+1} \quad (14)$$

in which:

$$|e_{n+1}| \leq |e'/d| + (e_n)^2 |d| + |e_n||e'| \quad (15)$$

Knowing that the maximum computational error, e' ($\leq 2^{-15}$), and the range of d (i.e., ½ to 1⁻), are both constants, we may substitute their worst case values into eq. 15 to determine the errors introduced by the implementation of the algorithm:

$$|e_{n+1}| \leq 2^{-14} + (e_n)^2 + |e_n| 2^{-15} \quad (16)$$

Since the second and third terms are second-order, with values which can be neglected, the maximum computational error contributed by each iteration is 2^{-14}.

Figure 6 is a plot showing the errors of 1000 equally spaced points over the normalized denominator range from ½ to 1, for a *single iteration* of the Newton-Raphson recursion using an 8-bit lookup and single-precision feedback, as shown in Figure 5. The rms error is about 39 parts per million, slightly more than 2^{-15}, while the maximum error for the set of points tested is 150 ppm. Since 2^{-14} = 61 ppm, and there are relatively few points with greater errors, we may conclude that the main source of error is the computational error introduced by the single-precision feedback term, e'.

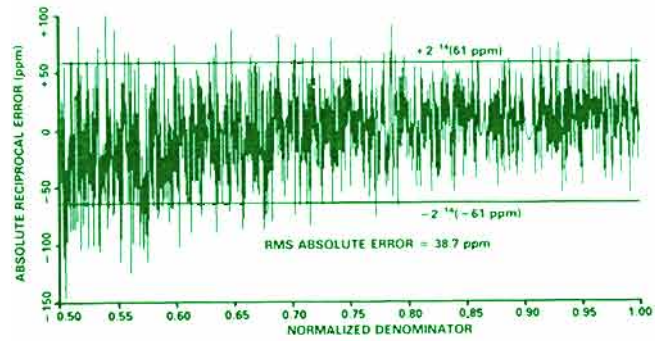


Figure 6. Absolute error for 16-bit reciprocal approximation.

We may also conclude that one recursion is generally adequate to obtain accuracies to better than 14 bits, and that the single-precision computational error, which degrades accuracy to the 14-bit level, insures that more than one iteration would not increase the accuracy. Although 14-bit accuracy is rather modest for many applications, remember that this whole computation is performed within 320 nanoseconds (2 × 145 ns for the multiplications + 30 ns for an ECL lookup table).

A SIMPLER IMPLEMENTATION

Until now, we have been assuming that all the multiplications have been performed in the unsigned arithmetic mode. A fortuitous identity in twos complement arithmetic allows us to simplify the hardware requirements of the reciprocal calculation:

A twos complement number is formed by taking the ones complement of a number and adding one LSB; it is equivalent to subtracting the number from the next higher power of 2. This suggests that perhaps the subtraction from 2 in (5) could be eliminated if the output of the multiplier were coded in 2s complement.

It may not be intuitively obvious, but we can eliminate the subtraction if we use the twos complement of the initial guess (call it y'_0) in forming the first product ($d * y'_0$)—and perform the multiplication in the "mixed" arithmetic mode (y'_0 in 2s complement and

d in unsigned), again using the format-adjust option of the multiplier (FA = 0). We get a single-signed, twos-complement product in the 1.15 format, which, if interpreted as an *unsigned* result, will in fact be the term $(2 - d*y_0)$. That is, when this result is fed back for the second multiplication, $y_0 (2 - d*y_0)$, we just clock it in as an unsigned number.*

It might appear that using this technique would require a double-size lookup table and an extra addressing bit for selecting between the twos complement and the unsigned values in the table of initial guesses. However, it turns out that we can avoid this.

Since there is strong evidence that the 8-bit ROM is more than adequate for the first guess, a 9-bit word to address a double sized, 8-bit lookup table needed to store both y_0 and y'_0 (which is not an available ROM configuration) is unnecessary. An initial guess, y_0, with greater accuracy than the computational error, avails us nothing. Thus we can reduce the number of segments used to derive the first guess by half, relegating the 8th bit to a bank-select function. With this technique, the error due to the initial guess (the quadratic term) will still be smaller than the computational error. Figure 7 shows a suggested hardware diagram.

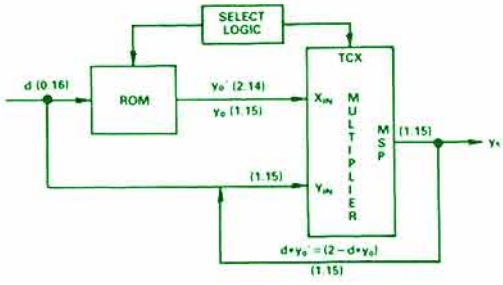


Figure 7. $(2 - d * y_0)$ in 1 operation with less hardware.

FURTHER SIMPLICITY WITH A SINGLE-PORT MAC

The ADSP-1110, a single-port, 16-bit multiplier/accumulator (MAC)—and much more—in a 28-pin package, is an unusually versatile new product from the DSP Division of Analog Devices. The ADSP-1110 has a 6-bit instruction set offering the user no fewer than 32 separate operations, while reducing the pin count for a 16-bit MAC function from 64 to only 28! Its salient features (Figure 8) include: a 40-bit accumulator, a pipelined input register, independent rounding control at bits 14 and 15, a left-shift output option, byte-swapping capability, an overflow flag, and saturation logic. The instruction set allows the user to form and accumulate products using any combination of addition, subtraction, and negation.

The Newton-Raphson reciprocal approximation can be implemented using the ADSP-1110 with simplified hardware. Although it was designed to excel in the multiply/accumulate (sum of products) mode, the device's internal bussing and left-shift option make it an attractive choice for recursive algorithms too.

By using the ADSP-1110 to implement the reciprocal, *either* approach $(2 - d * y_0$ or $d * y'_0)$ could be used in forming the first term. But again, the more expedient choice is the $(d * y'_0)$ which saves the implied overhead of preloading the accumulator with 2 in forming the difference term, $(2 - d*y_0)$.

In terms of layout, the 8th address bit will still be used to select either y_0 or y'_0, which may be provided by an extra instruction bit

*The proof of this, beyond the scope of this article, is available from the author upon request.

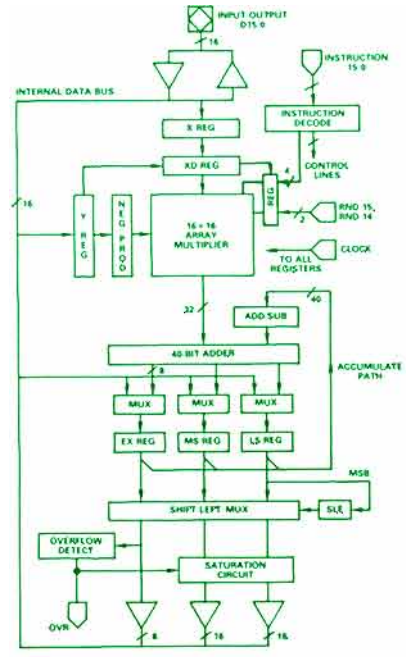


Figure 8. ADSP-1110 Single-Port MAC.

in the algorithm microprogram, but, except for that, the ADSP-1110 will do everything else inherently.

Consider the code sequence of figure 9. The first instruction loads the pipeline register with y'_0. The second simultaneously shifts the pipeline register, loads d, and starts the product in the mixed mode. Halfway through this multiply, the pipeline register is loaded with the first operand of the second multiply, after which the first product is latched. The fifth instruction outputs the result, which is then loaded into the Y register, starting the 2nd multiply of the MS and the shifted pipeline register. There being no more arithmetic operations to perform, the last 3 instructions are required to finish the recursion and output the reciprocal.

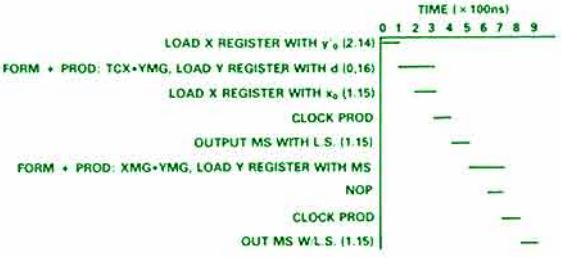


Figure 9. Code sequence to implement the algorithm with ADSP-1110.

Execution time (room temperature) for the discrete-multiplier implementation is 2 × 145ns + 30ns = 320ns (assuming 30ns for ECL ROM), or roughly 1/3 µs. The single-port MAC offers a simpler design, but it is almost three times as slow (900ns).

In these pages, we have investigated approximation technique (the Newton-Raphson recursion); we have learned how lookup tables are used in conjunction with normalized numbers for greatest dynamic range; and we have seen the use of 2s complement to combine a product and a difference term in one multiply—and its use in hardware implementation of reciprocals with high-speed multiplying devices. These approximation techniques, applicable to other scientific functions as well, for example logarithms, exponentials, linearizing functions, etc., serve to illustrate some unconventional—but useful—applications of digital multipliers.

75-MHz CONVERSIONS WITH 6-BIT MONOLITHIC FLASH ADC

Overflow Bit Allows Stacking of Devices for Higher Resolutions

AD9000SD Can Operate with Case Temperatures from −55°C to +125°C

by Don Brockman

The AD9000* is a 6-bit parallel a/d converter specified to convert at 75-MHz (min) word rates. Housed in a 16-pin ceramic DIP, it is available in two optional versions: the AD9000SD, for temperatures from −55°C to +125°C, and the AD9000JD, for applications in the 0°C to 70°C range. Prices (100s) start at $46.

A "flash" converter, it uses 64 parallel comparators to digitize fast-moving analog input signals without needing external track-hold (T/H) circuits. An overflow bit is provided for connecting multiple units in a stacked arrangement to obtain up to 8 bits of digital data at megahertz word rates. Figure 1 shows the input divider, comparator stages, latches, and encoders.

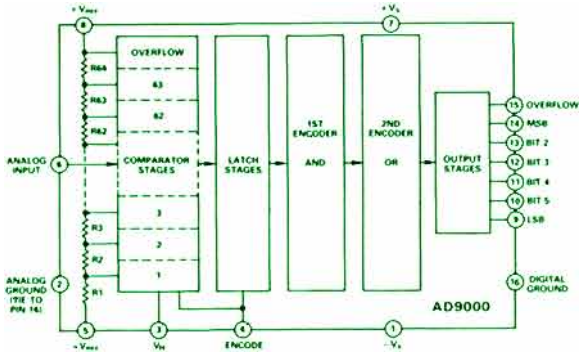


Figure 1. Block diagram of the AD9000.

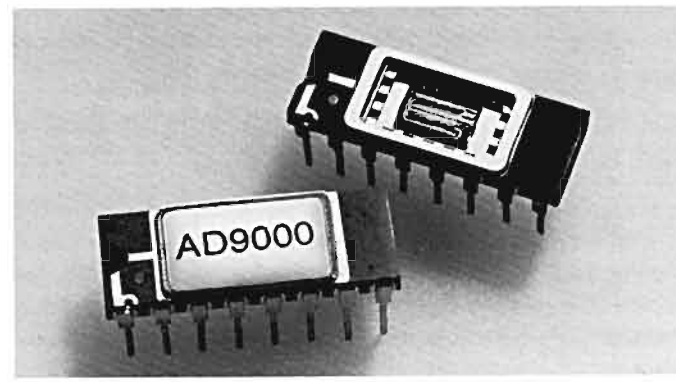
The input signal is compared with a set of 64 different reference voltages at equal 1-LSB increments, developed by a string of equal resistors connected between the positive (to +2 V) and negative (to −2 V) reference sources. The outputs of all comparators having inputs more positive than the reference are switched to logic "1"; the outputs of all other comparators remain at logic "0". Encoders provide the logic to encode the comparator decisions into a set of 6 parallel binary outputs, plus a carry to respond to overflow.

When the ENCODE input is low (0), the latches at the comparator outputs are transparent; the encoder inputs change state in response to changes in the output states of the comparators as they track the signal. When the encode input goes high (1), the latches go into "hold," retaining the last state of the comparators, with an aperture delay of about 2 nanoseconds and aperture jitter of about 25 picoseconds. When operating at 75 MHz, the encoder is assigned a "track" time of about 4 to 6 ns to acquire the next value of input and a "hold" time of 5 to 7 ns for the 6-bit output to reach a stable state, ready for latching.

APPLICATIONS

The AD9000 is used wherever fast-changing data must be acquired with appropriate resolution for storage, display, or processing. Areas of application include image processing, digitizing for video and radar equipment, and military systems. The AD9000 can also be used at the heart of special-purpose high-speed converters, including high-resolution (e.g., 10-13-bit) converters employing digitally corrected subranging (i.e., two-step conversion).

*Use the reply card for technical data.



As noted earlier, two or more 6-bit AD9000s can be employed to form converters having extended resolutions of 7 or 8 bits. This is accomplished by connecting the reference-resistor strings in series and the digital outputs in parallel. For 7-bit converters, involving 2 AD9000s, the reference inputs would be driven with high, low, and mid-scale reference voltages; for 8-bit converters, involving 4 AD9000s, the reference inputs would also be driven at the appropriate points by the quarter-scale reference voltages.

Figure 2 shows the connections for 7-bit conversion. The outputs for the six less-significant bits are wire-or'd together, and the MSB is produced by the overflow bit of the lower device. If the analog input to the cascaded arrangement is below half-scale, the OVERFLOW and all output bits of ADC #2 are zero; thus ADC #1 drives the 6 lower output lines. When the analog input is greater than half-scale, the OVERFLOW bit of ADC #1 is high and acts as a carry; all the digital output bits of ADC #1 go low, and ADC #2 converts the residual upper half-range—its outputs drive the output lines.

Since the conversions occur in parallel, there is no loss of speed, regardless of which converter's outputs are active. The MSB of ADC #2 is connected to circuitry insuring that, when overflow occurs, all output bits remain high rather than rolling over with the carry. ◘

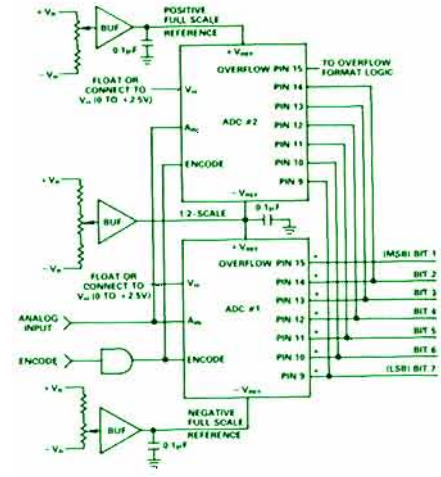


Figure 2. Connections for 7-bit conversion.

Application Note

RATE-OF-COOLING METER FOR CRYOGENIC APPLICATIONS

AD595 Thermocouple Amplifier Serves as Preamp and Hot-Junction Compensator

by Steve Kirby

This Note describes the design of an instrument that provides successful retention of physical integrity when biological specimens are frozen for imaging by a scanning electron microscope.

The scanning electron-beam microscope (SEM) is one of the most powerful tools in the research biologist's kit for probing the microstructure of plant and animal cells. An important factor that must be dealt with in preparing samples for SEM photography is the cell's water content. Comprising up to 90% of a cell's matter, the water content must be either removed or stabilized before the tissue sample can be placed in the high vacuum of an electron-beam specimen chamber.

Since removal of water in the liquid state leads to a distorting shrinkage, a better answer is to stabilize the water content by rapidly freezing the cell, then cracking it open to reveal the inner microstructure. Frozen water is etched away from the split surface to expose the complex sub-surface structure. Then the surface is coated with a thin layer of gold to make a shadow mask that the electron beam can "see" from the pattern of reflected electrons. A typical resulting photograph can be seen in Figure 1.

Figure 1. Fractured surface of well-frozen mushroom-gill tissue. Note the 20μm size reference.

The specimen must be cooled at the correct (fast) rate. If cooling is too slow, large ice crystals will form, totally destroying the beautifully ordered structure of the formerly living matter. Examples of the variety of cooling techniques available to biologists to remove the internal heat as quickly and evenly as possible include rapidly plunging the specimen into a bath of liquid propane and spraying the specimen with liquid nitrogen. By the use of a delicate micro-wire thermocouple—embedded in the tissue sample—to monitor temperatures, cooling rates of up to—10,000°C/s are achieved, resulting in ice crystals of almost imperceptible size.

The electron-beam micrograph procedure and the gold coating are expensive. If the cooling process doesn't work, the biologist is left with a costly photograph of a cell shattered by large ice crystals. (Figure 2). There was a need for an instrument to record the temperature of the specimen over the cooling period and, using the

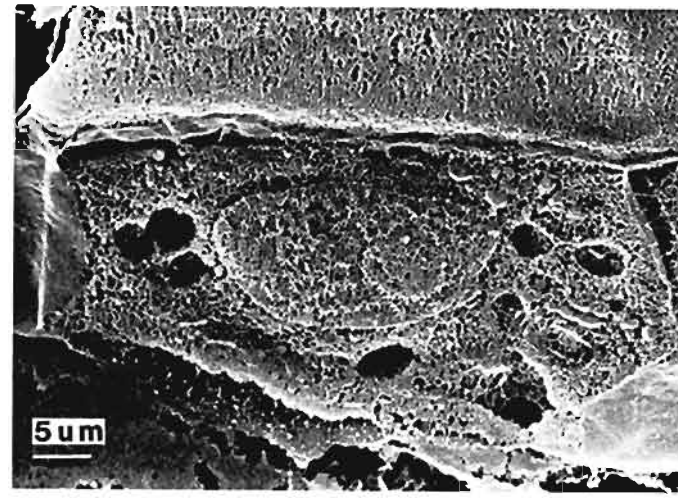


Figure 2. Section through the etched surface of a poorly frozen cell, showing ice-crystal artifacts.

data, to calculate the average rate of cooling—a figure of merit that could be used to decide whether to abandon the remaining steps.

The Cryometer 100K (Figure 3), an instrument with these—and many other—capabilities, was developed for the Centre for Cell and Tissue Research in the Department of Biology at the University of York, England, by the York Electronics Centre.

THE CRYOMETER 100K

The Cryometer, designed around a Zilog Z8 single-chip microcomputer, controls a dedicated transient recorder which samples the amplified micro-wire thermocouple signal at regular intervals, from 100 ms down to 100 μs. A 16-character alphanumeric liquid-crystal display provides clear user-friendly messages to the operator, who sets up and runs the Cryometer from a keypad. Its objectives were to be accurate, cheap, robust, foolproof, and small!

Figure 3. The Cryometer 100K.

The block diagram of Figure 4 shows how the Cryometer works. The thermocouple and its amplifier, start-stop threshold circuitry, and data-acquisition circuits are at the left; the μP, keypad, and display are at the top; the logic and transient-recording sample

memory are at the right, and the outputs to an optional analog recorder are at bottom.

The AD595 thermocouple amplifier* provides a temperature reference, microvolt-level amplification, and open-thermocouple indication. Since thermocouples only measure the *difference* between the temperatures at their hot and cold junctions, the "inactive" junction (often called the "cold" junction, but in this case the hot junction) must be kept at a constant temperature, usually 0°C, to provide a reference for the measurement. Since the ambient at the instrument is generally neither 0°C nor constant, a voltage corresponding to the difference between the instrument's temperature and 0°C must be subtracted from the thermocouple reading.

The AD595 performs this function by subtracting a voltage corresponding to its own Celsius temperature (which must be close to that of the "ambient" thermocouple junction), with a sensitivity equal to that of the thermocouple type being used, thus effectively creating a 0°C hot-junction reference. The AD595 then amplifies the difference up to a convenient 10 mV/°C level. With this scaling, the Cryometer's −200°C to +35°C range fits nicely into the the range of an a/d converter with a standard 2.5-V reference.

An attractive feature of the AD595 is the small amount of real estate it occupies on the 7" × 8" circuit board (at upper left, Figure 5). Although the AD595 is precalibrated for Type K (iron-constantan) thermocouples, its gain can be adjusted to match the sensitivity of Type T thermocouples used in cryogenic thermometry. The very fine (38 swg) thermocouple wire sometimes breaks under cooling stresses; when this happens, the incident is detected by the AD595, which causes a warning to appear on the LCD display.

Often the biologist is interested in only the portion of the cooling curve between arbitrarily set *start* and *stop* thresholds (Figure 6). This is easily set up by keying in the temperatures at which data logging will start and stop. Voltages corresponding to the threshold temperatures are set digitally as inputs to an AD7528 dual 8-bit DAC. The outputs of the DACs and the amplified thermocouple voltage are compared in two comparators; their state controls the arming and trigger logic.

The output of the AD595 is level-shifted, for compatibility with the a/d converter, and filtered before being converted. As the specimen rapidly cools, the 8-bit output of the ADC is stored in the transient-recorder section of the Cryometer, a 2K by 8-bit CMOS RAM. Only those temperatures within the window established by the start-stop thresholds are logged.

The AD7528 is especially useful here for several reasons. First, the close tracking of the two DACS (on a single monolithic chip) allows the user to choose a narrow window in the middle of a large cooling-temperature range and be sure that the separation will be stable. In addition, considerable space is saved by having two DACs and their data-holding registers in one 16-pin DIL package.

*For technical data, use the reply card.

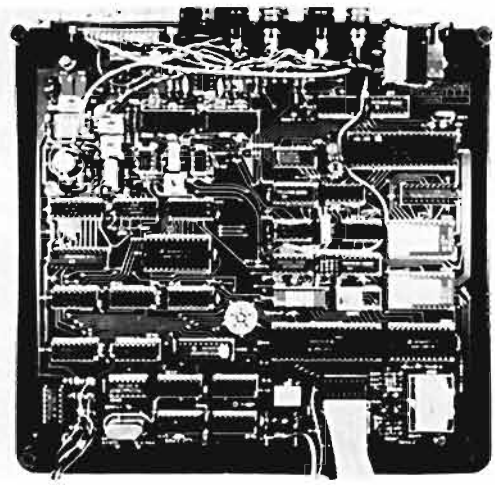


Figure 5. Photo of PCB layout of the Cryometer.

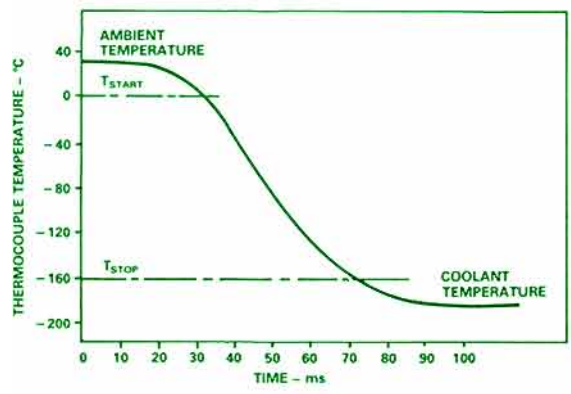


Figure 6. Typical cooling curve.

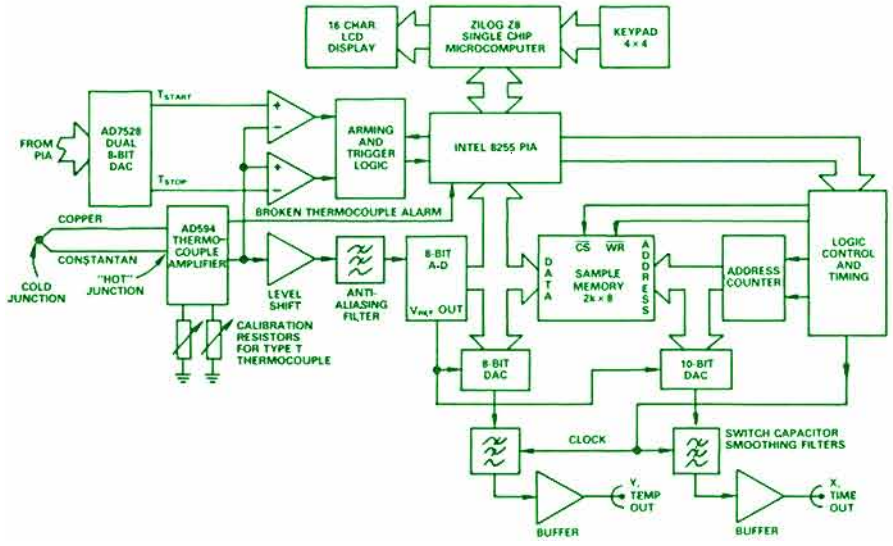


Figure 4. Block diagram of the Cryometer.

The Z8 can read back the temperatures, calculate a fitted straight line and its slope, and display it when the appropriate key is pressed. Individual points can be called back for examination, and the whole record may be sent off to a larger computer for further processing.

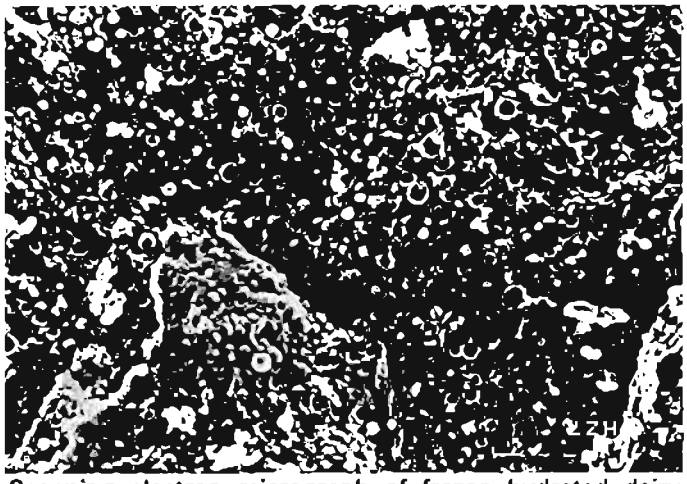
Two output DACs, a 10-bit DAC for time, and an 8-bit DAC for temperature, are used to provide an immediate picture of the cooling curve; it can be displayed on an oscilloscope, and an X-Y plotter may be used for hard copies. Switched capacitor low-pass filters are used on the DAC outputs to smooth out the steps; since the −3dB frequency is set by a TTL clock input from the Z8, a wide range of replay frequencies are available.

Thermocouples are inherently nonlinear—and often more so at low temperatures. For example, the sensitivity of Type T varies from about 15 to 40 μV/°C over the −200°C to +35°C range. In the computerized system, this variation can be almost entirely corrected by having a lookup table of 256 true temperature values corresponding to each of the measured temperature values. The table contents can be laboriously plugged in point by point or derived from a polynomial fitted to standard thermocouple characteristics published by the National Bureau of Standards.

A subtle calibration point: As noted earlier, the AD595 is pre-calibrated (laser-trimmed on the wafer) for Type K thermocouples. For 10 mV/°C sensitivity with Type T, the gain must be recalibrated, by the procedure noted in the AD595's instructions. When this is done, the value of the EMF/temperature slope must be chosen for the actual temperature at which the AD595 will be operated—and it may be higher with the instrument case closed than with the case open. The thermocouple's nonlinearity can cause an error of several degrees for the unwary!

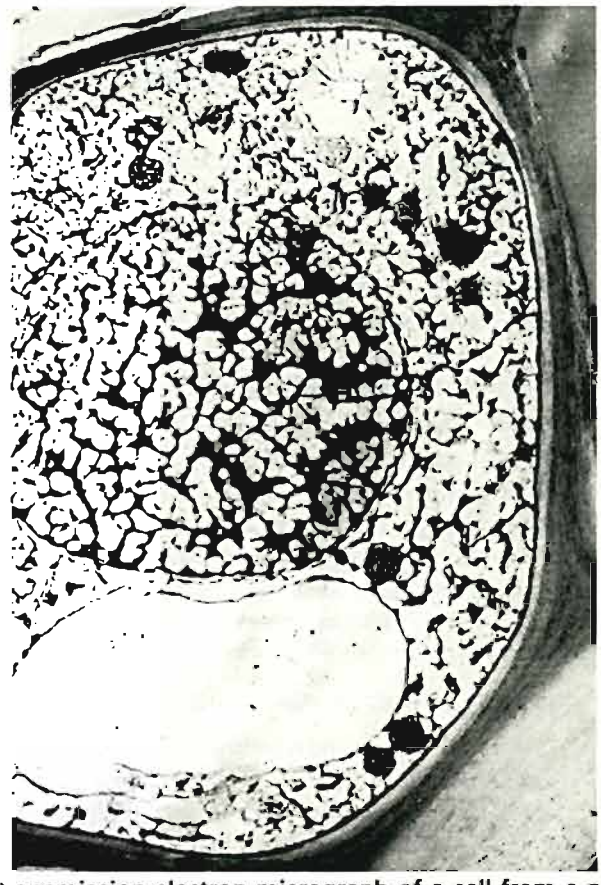
EXAMPLES OF ELECTRON-BEAM MICROGRAPHS

These photographs[1], taken in the electron microscope, demonstrate the effects of specimen cooling-rate on the final image obtained in electron-beam micrography.



Scanning electron micrograph of frozen hydrated dairy cream (temperature of the sample in the electron microscope is about −160°C) demonstrating spherical lipid droplets in an aqueous casein matrix. The specimen has been 'cryo-fixed' by very rapid cooling, thereby eliminating large structure-destroying ice crystals.

SEM photo of frozen hydrated pollen grains on the stigma of the garden flower, *Alyssum* (same temperature as in the example above). Again, the cooling rate was rapid and ice crystals are small, giving rise to little structural damage.



A transmission electron micrograph of a cell from a plant root, prepared by freezing. In this case, the cooling rate was slower than in the cases mentioned above, and ice-crystal growth is considerable, giving rise to the lace-curtain appearance (also seen in Figure 2). Large electro-lucent voids (holes) can be seen in the tissue where the ice crystal had grown, forcing the darkly stained cell-sap into a eutectic around the crystal. It can be seen that crystals are larger in some cell structures than in others.

[1]We are grateful to Mr. Ashley J. Wilson, Manager of the Centre for Cell and Tissue Research, Department of Biology, University of York, for providing the above photographs, and to Mr. Graham Long, Manager of the York Electronics Centre, for encouragement and permission to publish the article about the Cryometer 100K. For further information on the instrument, write to

Manager, York Electronics Centre
University of York,
Heslington, York YO1 5DD
United Kingdom

MONOLITHIC CMOS TRIPLE-OUTPUT DC-DC CONVERTER

AD7560 Provides −5 V and −15 V Supplies, −10V Reference, All from +5V Supply
Latchup and Short-Circuit Protected, 16-pin Plastic DIP, Only $4.75 (100s)

by Hans Tucholski and John Wynne

The AD7560* is the first monolithic CMOS dc-to-dc converter with multiple supply outputs, converting a positive supply voltage, $+V_{DD}$, to $-V_{DD}$ and $-3 \times V_{DD}$. In addition, it provides a negative reference voltage that has a low temperature coefficient and high power-supply rejection (Figure 1).

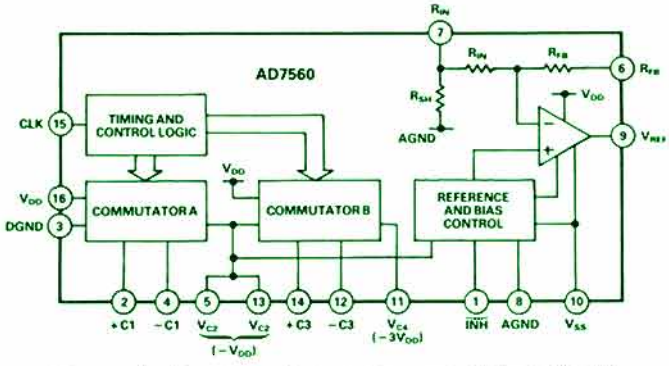


Figure 1. Functional block diagram of the AD7560.

Designed for efficient, economical, reliable operation, it works with as few as 2 capacitors and is protected against damage due to latchup and short circuits. Furnished in a plastic 16-pin DIP, The AD7560JN has an operating temperature range of −25°C to +70°C and a price of only $4.75 in 100s.

Its uses include: generating negative reference voltages for data acquisition in systems having a single +5-volt supply; generating negative supply voltages for low-power op amps, analog switches, ADCs, DACs, etc.; and low-power high-efficiency conversion for single-battery operation, eliminating replacement of costly multiple batteries. The AD7560 may also be used as a multiple remote voltage source in applications where wiring is at a premium.

WHAT IT DOES

The AD7560 provides logic and repetitive switching, transferring charge to and from a pair of external capacitors in the proper sequence to provide an output that is nearly equal to the input voltage but of opposite polarity, $V_{C2} = -V_{DD}$ (Converter A). A second circuit (Converter B), using an additional pair of capacitors, operates similarly to provide voltage doubling and augmentation; this results in voltage tripling ($V_{C4} = -2V_{DD} - V_{DD} = -3V_{DD}$). In addition, the unregulated $-3V_{DD}$ output from Converter B is used to generate an internal reference voltage of −5 V, which—buffered and amplified—provides a temperature-compensated −10 V reference output capable of sinking at least 1.0 mA.

The converters can be driven by a free-running on-chip oscillator at a frequency determined by an external capacitor; or, for applications where synchronization is needed, the clock input can be driven directly from a 5-V CMOS-compatible clock source.

With a +5-volt supply, the −10-volt reference has a maximum initial tolerance of ± 0.5 V, maximum tempco of ± 200 ppm/°C, maximum power-supply rejection of ±12 mV/V, and maximum output resistance of 3 ohms. When the reference circuit is not needed, a logic signal ($\overline{INH}$) permits it to be powered down, reducing the load on the supply outputs.

Supply A has a minimum voltage-conversion factor ($-V_{C2}/V_{DD}$) of 0.85 and maximum output resistance of 200 ohms, over the temperature range; Supply B has a minimum conversion factor ($-V_{C4}/V_{DD}$) of 2.75 and maximum output resistance of 1200 ohms over temperature. The voltage-conversion factors of each supply are substantially affected by loading of the other supply and enabling of the reference circuit.

APPLICATIONS

Principal applications of the AD7560 are in generating local negative voltages. For instance, most single-board microcomputers require only +5-V supplies. If data-conversion capability is to be added, and bipolar analog signals must be processed, a negative voltage supply will be required. Usually, just a small number of components (input ADC, output DAC, low-power op amps) need negative supplies, and then only in small amounts. The AD7560 is a cost-effective single-chip way of avoiding the design or purchase of conventional auxiliary power-supply capacity.

Figure 2 shows the generating principle and external circuit connections required to generate a nominal −5 V from a +5-volt source. Capacitors C1 and C2 are 10-μF/10-V low-cost electrolytics. The converter oscillation frequency is controlled by C_{CLK}; a 1 nF capacitor produces a clock frequency of about 6 kHz.

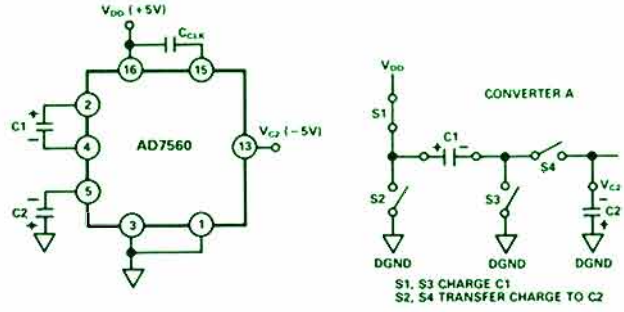


Figure 2. AD7560 connected to generate −5V.

Figure 3 shows the circuitry required to generate a nominal −15 V from a +5-volt source. Capacitors C3 and C4 are 10 μF/25 V low-cost electrolytics.

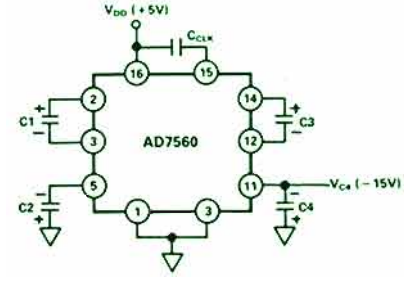


Figure 3. Connection for −15-volt range.

*Use the reply card for technical data.

Figure 4 shows how the circuit of Figure 2 can power a digitally controlled attenuator for bipolar ac input signals of up to ± 5V, employing an 8-bit CMOS DAC, the AD7524, for 2-quadrant multiplication. The DAC coding is unipolar binary, for gains from 0 to $1 - 2^{-8}$.

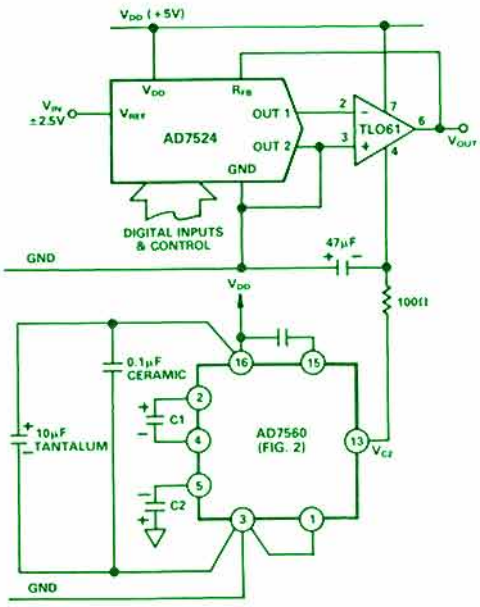


Figure 4. AC attenuator with bipolar output.

Since the AD7560 works by essentially pumping charge from one capacitor to another in synchronization with the clock frequency, (pin 15), one can expect that the clock frequency will be present as noise spikes on the generated output voltages. Noise spikes will also be reflected back to the supply via the V_{DD} input.

To keep these noise spikes to a minimum, pay careful attention to the circuit wiring. As Figure 4 indicates, the power and ground lines to the AD7560 should—to the degree possible—be returned separately to the power supply. The DAC and op amp are supplied via separate lines. Note also that the R-C filter for the V_{C2} output is referred to the DAC ground, not the AD7560 ground. With these simple precautions, the noise spikes in the vicinity of the DAC circuit can be appreciably reduced. Figure 5 shows the noise breakthrough on the op-amp output when employing these guidelines.

Figure 5. Reduced noise spikes in the circuit of Figure 4; vertical scale, 5 mV per division.

Figure 6 shows the AD7524, with a fixed reference, connected in the voltage mode (reversing the current-mode input and output connections[1]), to obtain a ± 1.2-V output voltage range. Offset-binary coding is used; The MSB is inverted for 2's complement.

[1]See "CMOS DACs in the Voltage-Switching Mode," *Analog Dialogue* 14-1, 1980, pages 16-17.

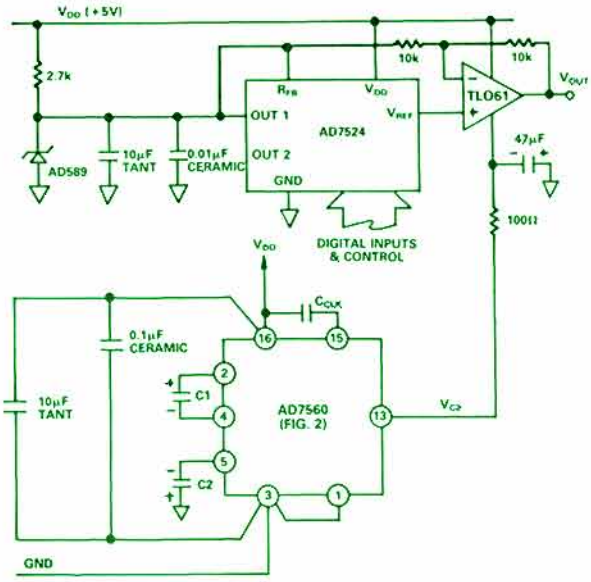


Figure 6. Digitally adjustable voltage source with bipolar output.

When applications call for accuracies beyond 8 bits and long-term stability beyond the AD7560's capability, the AD7560 can be configured to drive an AD584 reference, to generate a high-precision − 10V reference for loads of up to 1.0 mA. A circuit to perform this, using the V_{C4} output, is shown in Figure 7. The wiring guidelines mentioned above should be adhered to.

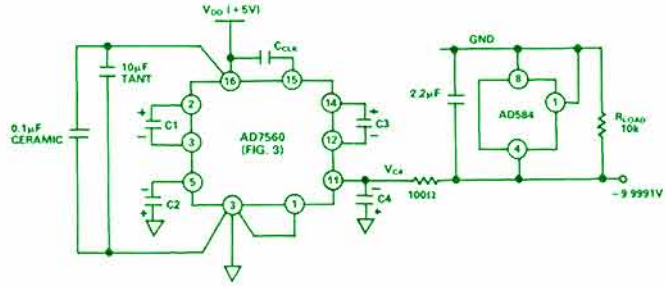


Figure 7. Generating a high-precision − 10-V reference.

The AD7560 can be used in a temperature-monitoring circuit employing the AD590 or AD592 (see page 29) semiconductor temperature sensor (Figure 8). Output sensitivity is 10 mV/°C, giving a positive 0 to + 1-volt range for a temperature range from 0 to 100°C. Trim the circuit by adjusting RV1 for 0 V output with the AD590 at 0°C and RV2 for + 1.00 V output with the sensor at + 100°C. Op amps A1 and A2 should be low-power devices.

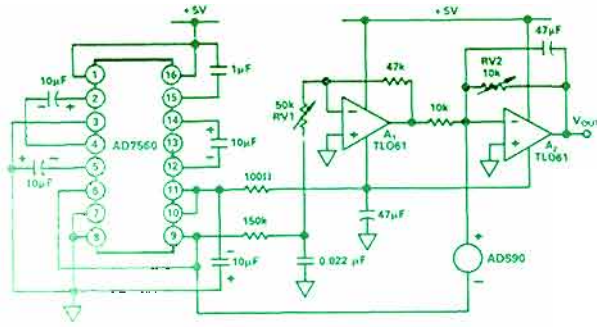


Figure 8. Temperature-monitoring circuit.

COMPLETE MONOLITHIC 8-BIT, 10-μs A/D CONVERTER

AD670 Is Fully μP-Compatible, Accepts Low-Level Differential Analog Signals Completely Self-Contained, It Operates from +5-Volt Computer Supplies

by Doug Grant, Diane Heerema, and Doug Mercer

The AD670 "ADCPORT",* the near-ideal 8-bit ADC, is a complete, microprocessor-compatible easy-to-use a/d converter on a single monolithic chip. A successive-approximation device, it contains its own buffer amplifier, voltage reference, d/a converter, latching comparator, successive-approximation register, 3-state output latches, and control logic. It performs a complete conversion in 10 μs, operates from a single +5-volt supply, and, because it is packaged in plastic, it's low in cost. Prices are under $6 in 1000s.

Housed in a 20-pin DIP, it combines innovative circuits, precision bipolar processing, and laser-trimming at the wafer stage to eliminate the need for external gain or offset trims. Integrated injection logic (IIL) makes possible high-density packaging of both high-speed digital logic and low-level analog circuitry on a single chip.

WHAT IT IS

In 1980, we introduced the AD558 DACPORT (*Dialogues* 14-1 and 14-2) to our readers; it achieved instant popularity. It is a complete 8-bit μP-to-voltage converter, requiring only a single supply and designed for easy interfacing to digital input, analog output, and the power supply. The AD670 is the a/d counterpart of the DACPORT—an ADC that is easy to deal with at all interfaces—analog, digital, power, and human.

Figure 1 is a functional block diagram of the AD670, showing the relationship of its various parts. Although most of them appear to be fairly typical of successive-approximation ADCs, there are noteworthy features important to an understanding of the applications of the device—the instrumentation/buffer amplifier and the control section (which includes logic-controlled format and polarity)—plus a few other features that are simply worth knowing about.

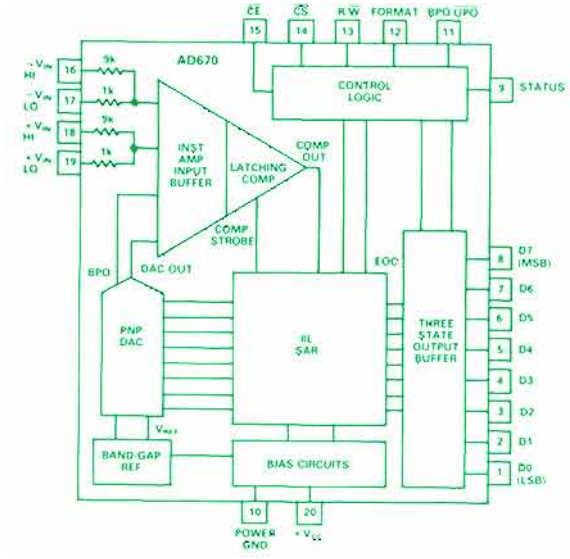


Figure 1. Block diagram of the AD670.

*Use the reply card for technical data.

When conversion starts, the input signal, buffered by the amplifier, is compared with the output of the DAC; the MSB is set high. If the input is less than one-half the span, the MSB is returned low; if the input is greater, the MSB remains high. The next bit goes high, and the input is compared against either ¼ or ¾ span (depending on whether the MSB is low or high). Again, a decision is made and the following bit goes high. Trials and decisions continue until the last bit has been exercised. When a *read* is requested, the data is read out via the three-state latches.

Instrumentation amplifier. Perhaps the most unusual feature of the AD670 is the differential-input instrumentation amplifier. This front end offers the user a choice of pin-programmable resolutions, 1 or 10 millivolts per bit (255 millivolts or 2.55 volts full-scale span). It makes possible the designer's dream, a converter with a single supply that can be wired directly to a low-level transducer—such as a strain gage or load cell—in (if desired) a converter-per-channel system.

Each of the differential inputs of the instrumentation amplifier is connected to two terminals, one via a 1 kΩ resistor, the other through a 9 kΩ resistor, in a precisely trimmed ratio. As Figure 2 shows, the connections can be (a) strapped together for low-level differential signals, (b) connected for attenuation of high-level

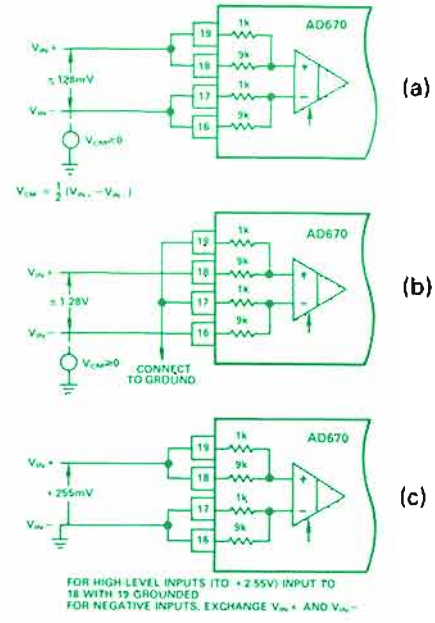


Figure 2. Analog input connections. (a) Low-level differential. (b) High-level differential. (c) Low-level single-ended.

differential inputs, or used single-ended with the low side grounded (c). Thus, signals of either polarity may be handled accurately, as long as the lower of the two voltages is more positive than −128 mV *at the amplifier*.

The instrumentation amplifier also buffers the signal source from the conversion circuitry. This feature will be appreciated by any engineer who has had to contend with the loading problems

caused by rapidly changing currents at the input of a current-summing successive-approximation ADC. While the series resistors provide attenuation when needed; they also offer latchup-free overrange protection against momentary shorts to voltages up to + or − 30V. This applies to either input and either gain range.

Microprocessor Interface. Besides the eight high-speed, three-state-buffered data outputs, the digital connections of the AD670 include a STATUS output (which indicates when conversions are in progress), and 5 control inputs, which are compatible with TTL, LSTTL, and 5-V CMOS logic. The control inputs include a chip-select ($\overline{CS}$), chip enable ($\overline{CE}$), read/write (R/$\overline{W}$), FORMAT—binary or 2s complement coding, and BPO/$\overline{UPO}$—bipolar/unipolar analog range.

The FORMAT and BPO/$\overline{UPO}$ inputs can be either hard-wired to the appropriate logic level or independently software-programmed for each conversion. When inputs having mixed unipolar and bipolar input ranges are multiplexed, each input can be programmed in its turn to be represented in the appropriate digital format.

The AD670 looks to the microprocessor like read/write memory. The μP can initiate conversions by bringing R/$\overline{W}$, $\overline{CS}$, and $\overline{CE}$ all low. At the same time, at the beginning of a *write* (start conversion), the states of the FORMAT and BPO/$\overline{UPO}$ input lines are latched into the converter and affect the conversion then under way. If these control inputs are connected to two data-bus lines, the μP can write updates into them for each conversion.

Within 700 ns after a conversion is initiated, the STATUS line goes high and does not return low until the conversion is completed; while STATUS is high, the chip will ignore all control inputs. After the conversion is complete, the μP can read the results by bringing $\overline{CS}$ and $\overline{CE}$ low, while R/$\overline{W}$ is high, to place the results of the conversion on the data bus. The STATUS can be used to initiate an interrupt to inform the CPU that the conversion is completed. The timing relationships for the *write* and *read* cycles are indicated in Figure 3.

APPLICATIONS

The AD670 can be used for almost any 8-bit (or wider) bus application for which an 8-bit signal-conditioning ADC, with 10-μs conversion time, is suitable. It is the natural answer to the question, "Which 8-bit ADC shall I use?"

Figure 4 shows a circuit application in which the output of a load

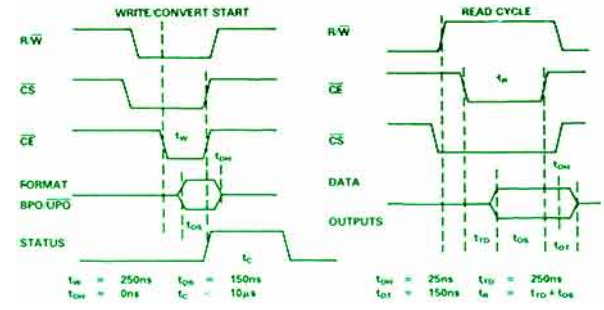


Figure 3. Timing diagrams for CONVERT and READ.

cell must be digitized. The load cell is driven from a buffered AD584 reference, connected as a ±2.5V tracking reference; and the differential output of the load-cell bridge is applied to the inputs of an AD670.

The example also shows how easy it is to interface the AD670 directly to a computer—in this case an APPLE. In the program listing of the subroutine that interfaces the AD670 to the computer, Figure 5, the converter is configured for a bipolar input range and offset-binary coding by the POKE instruction to the base address of the APPLE's Slot 5 (line 681), which also starts the conversion cycle. Since the AD670 converts in 10 μs, the result can be read by PEEKing into the location which contains the converter (line 690) immediately after the POKE ("immediately" means a 1-ms delay in BASIC on the APPLE). In the interest of reducing possible noise, 100 readings are averaged. This doesn't slow the program down significantly for human perceptions. ■

```
1  PR# 1: PRINT  CHR$ (9);"47N": LIST :  130  PRINT "NET WEIGHT IS "INTWT;"
     PR# 0: END : REM       HARDCOPY          POUNDS."
     OF LIST PROGRAM IN APPLESOFT          140  PRINT : PRINT : PRINT
2  REM    TO INTERFACE AD670 8-BIT          150  GOTO 110
3  REM    ADC TO DATA INSTRUMENTS           670  REM    THIS ROUTINE INTERFACES
4  REM    JP-20 LOAD CELL WHICH HAS         671  REM    THE AD670 TO THE APPLE AND
5  REM    +/-150 MV OUTPUT FOR              672  REM    AVERAGES 100 READINGS, THEN
6  REM    +/-2.5 VOLT INPUT.                673  REM    CONVERTS THE ANSWER TO LBS
7  REM   +/-2.5 VOLT INPUT.                 675 W = 0
10  PRINT : PRINT : PRINT : PRINT          680  FOR I = 1 TO 100
20  PRINT "TARE (T) OR WEIGH (W)? ";       681  POKE 49360,2 REM    THE '2' SETS
30  INPUT A$                               682  REM    THE AD670 FOR OFFSET-
40  IF A$ <> "T" THEN  GOTO 100            683  REM    BINARY OPERATION
50  PRINT : PRINT "CLEAR SCALE NOW"        684  REM   AND BIPOLAR INPUT
60  FOR I = 1 TO 1000: NEXT I              690 X =  PEEK (49360) REM    TO READ
70 TARE = W                                691  REM    OUTPUT AFTER CONVERSION
80  PRINT "TARE IS "ITARE;" POUNDS"        695 X = X - 128
90  PRINT : PRINT : PRINT                  700 X = (X / 150) * 20
95  GOTO 20                                710 W = W + X
100  REM   ACTUAL WEIGHT ROUTINE           720  NEXT I
105  PRINT "PUT THE OBJECT ON THE          730 W =  INT ((W / 10) + 0.5)
     SCALE."                               740 W = W / 10
110  GOSUB 670                             750  RETURN
120 NETWT = W - TARE                       1000  END
125  PRINT : PRINT : PRINT : PRINT
```

Figure 5. Data-acquisition subroutine.

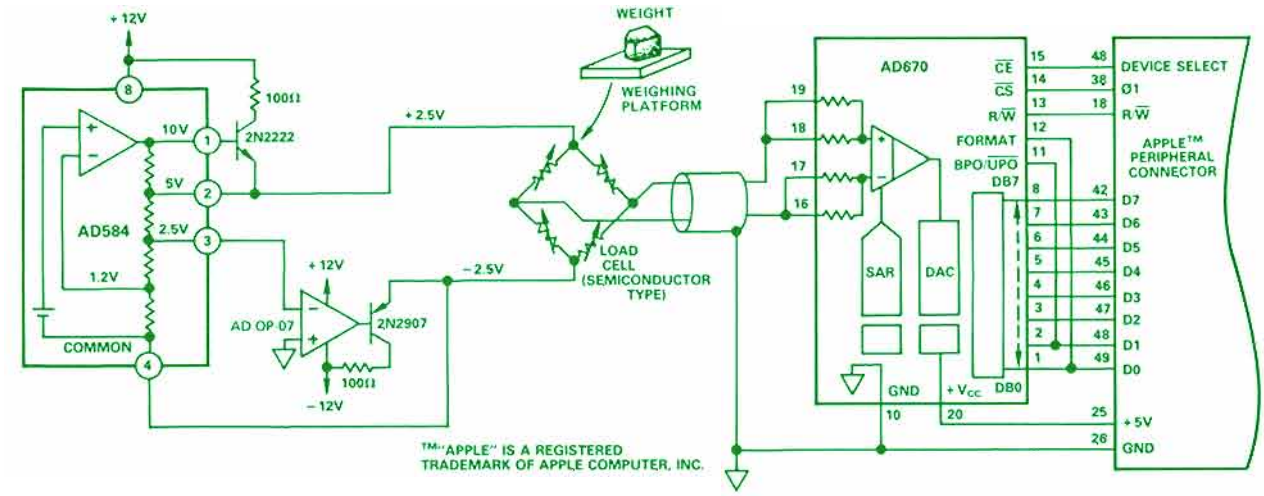
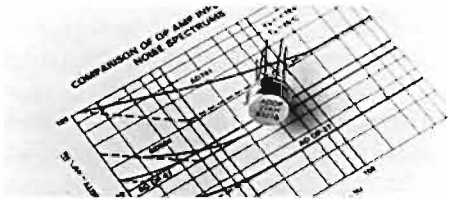


Figure 4. Interfacing to a bridge-type load cell and an APPLE computer.

New Product Briefs

LOW-NOISE OP AMP

0.18 μV p-p max for AD OP-27
Low Cost in Plastic Mini-DIP



The monolithic AD OP-27* operational amplifier, combining maximum low-frequency input noise of 0.18 μV peak-to-peak† with maximum offset voltage & drift of 25 μV & 0.6 μV/°C, and maximum long-term drift of 1.0 μV/month (A and E versions), is an alternate source to the industry-standard OP-27.

In addition to its low drift and noise, it has good dynamic performance, with a minimum gain-bandwidth product of 5 MHz, internally compensated, and a slewing rate of 1.7 V/μs, minimum. Combining these characteristics with its low ac noise, 3.8 nV/root Hz (max) at 1 kHz†, it is the definitive choice for applications involving precision handling of ac signals.

Low input bias and offset currents (35 nA and 40 nA max) allow the AD OP-27 to maintain good accuracy over a wide range of source impedance. These characteristics, in conjunction with a minimum CMR (common-mode rejection) of 114 dB (A and E) and minimum open-loop gain of 10^6†, well-suit the AD OP-27 for low-level signal amplification in instrumentation applications.

Pin-compatible with other bipolar op-amp types (OP-07, OP-05, OP-06, 5534, 725, 714, and 741), it will upgrade existing designs.

There are 6 performance grades for two temperature ranges. From −25°C to +85°C, G/F/E grades (available in hermetically sealed TO-99 metal can or 8-pin mini-DIP) specify maximum offset voltage and drift of 100/60/25 μV and 1.8/1.3/0.6 μV/°C. The same specifications are guaranteed for the C/B/A grades (in TO-99 only) from −55°C to +125°C. Prices (100s) are from $3.85 for the AD OP-27GN to $48 for the AD OP-27AH. ◘

*Use the reply card for technical data.
†A, B, E, and F versions.

MONOLITHIC TEMPERATURE SENSOR

AD592 Has Linear 1 μA/K (1 μA/°C) Current Output
Price<$1.00, Housed in TO-92 Plastic Package

The AD592* is a 2-terminal monolithic IC temperature transducer with output current proportional to absolute temperature from −25°C to +105°C. It is an easy-to-use sensor in a plastic package, for appliance, automotive, industrial, energy-mangement, and equipment-monitoring applications.

Its linear response—a 1 μA/K slope—makes the AD592 especially easy to use, eliminating the linearizing circuitry, cold-junction compensation, and bridge components that are typically needed in thermocouple, RTD, and thermistor installations. It is practically insensitive to excitation voltage and will operate with voltages from +4 to +30V.

In addition, current output eliminates errors due to line drops and induced voltage noise in long leads. With a single twisted pair, the AD592 will transmit a temperature signal more than a hundred meters (several hundred feet) and produce a full-scale change of 1.3 volts in a 10-kilohm resistor, corresponding to a 130°C temperature change at the source.

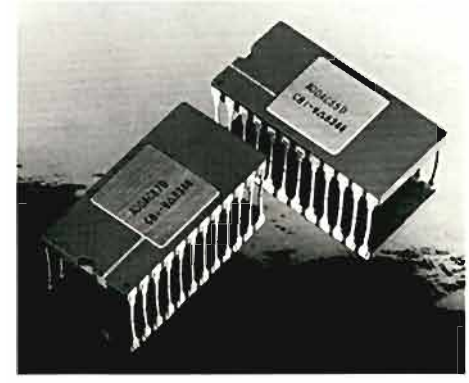
Laser-trimmed for better accuracy and interchangeable, AD592 units are available in three accuracy grades, AN/BN/CN. Full-scale accuracies are to 3.5/2.0/1.0°C of the correct absolute temperature (kelvin) for the −25°C to +105°C range, and somewhat better from 0°C to +70°C. Maximum nonlinearities are 0.5°C/0.4°C/0.35°C.

The AD592 is designed for low-cost, high-volume applications; its price is low. AN/BN/CN are priced at $2.95/$5.95/$9.95 in 100s and $.95/$1.90/$3.80 in 10,000s. ◘

MONOLITHIC 12-BIT D/A CONVERTER FAMILY

AD DAC80, AD DAC85, and AD DAC87 – Better Second Sources
One-Chip Devices with Voltage- or Current-Output Options

To begin with, the AD DAC80*, AD DAC85*, & AD DAC87* family of 12-bit voltage-output DACs (including a current-output version of the DAC80) are form, function, and spec compatible with monolithic and hybrid devices bearing the same industry-standard names; i.e., 12-bit internally referenced DACs with complementary binary coding.



They run cooler, offering 30% less dissipation than the closest competitor, and consequently the highest predicted MTBF (mean time between failures), of any similarly designated device currently on the market. Manufactured in accordance with MIL-M-38510, Class B, the AD DAC85 and AD DAC87 have calculated MTBF of 161,000 hours (ground-benign conditions). The DAC87 is offered to DESC drawing 83003.

In addition, performance is improved. For example, the current-output AD DAC80D-CBI-I is laser-trimmed at the wafer stage for full-scale output span of 2 mA ±2%, eliminating the need for adjustment in many applications. Voltage-output devices have the fastest settling time, 3 μs maximum to ±0.01% for a 10-V full-scale change.

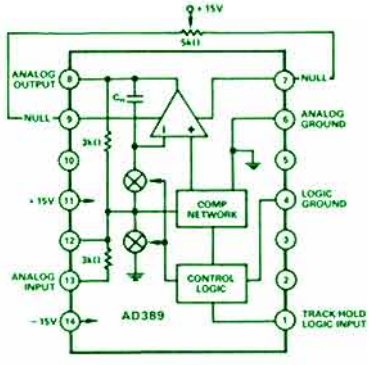
Other important advantages: They don't need a +5-V supply, and they will operate with either ±12V or ±15V supplies; thus, a "Z" option is not needed. They will upgrade performance or reduce cost of equipment originally designed for devices employing the standard pinout. For example, you can reduce cost with AD DAC80N-CBI-V, housed in a reliable plastic package. Device prices start at $15.50 (AD DAC80D-CBI-I, 100s). ◘

HIGHEST-RESOLUTION, -SPEED, TRACK-HOLDS

First Hybrid 14-Bit Track-Hold

AD389's Acquisition Time is 2.5 μs to ± 0.003%

The AD389* is a high-accuracy adjustment-free track-and-hold amplifier, complete with internal hold capacitor, in a 0.3" hermetically sealed DIP. Designed as a companion for high-resolution converters in data-acquisition, it has a fast acquisition time (2.5 μs to within 300 μV of final value) and low aperture jitter (400 ps), suitable for digitizing signals at up to 40 kHz with fast high-resolution ADCs.



*Use the reply card for technical data.

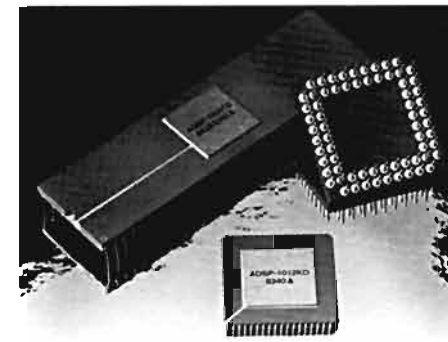
It also has a low droop rate of 0.1 mV/ms, providing the necessary combination of fast acquisition and long holding to avoid loss of accuracy with low-speed ADCs.

Typical applications include sampled-data systems, peak-hold functions, strobed measurement systems, and simultaneously sampled conversion. With a high-linearity ADC in a system employing autozero and autocalibration, it offers the possibility of 14-bit performance over the converter's entire no-missing-codes temperature range.

Configured as a unity-gain inverter, it is available in "K" and "B" versions for 0° to +70°C and −25°C to +85°C. Prices start at $74 (100s).

CMOS ICs FOR DSP

12 × 12 Multiplier and Multiplier-Accumulator



The ADSP-1012* is a CMOS 12 × 12-bit digital multiplier, and the AD1009 is a CMOS 12 × 12-bit multiplier-accumulator (MAC). They are extensions to the popular ADSP-1000 family of high-speed, low-power multipliers and MACs.

Like 16 × 16-bit devices announced in earlier issues of *Analog Dialogue*, they are pin-for-pin replacements for devices now on the market—in this case, the MPY-12HJ and the TDC1009J; they offer comparable speed while dissipating only 1/20 of the power.

Multipliers and MACs are used in such digital signal-processing functions as correlation, digital filtering, fast Fourier transformations, and matrix multiplication, for high-end graphics and simulation systems, transmultiplexers, high-end modems, radars, artificial vision-pattern recognition systems, medical imaging equipment, array processors, etc.

Dissipating maximum power of 150 mW at a 6-MHz clock rate, the ADSP-1012 and ADSP-1009 are specified to have maximum cycle times of 110 ns and 130 ns at +25°C. K and T grades of the ADSP-1012 spec 130 ns and 150 ns cycle times over their 0°C to +70°C and −55°C to +125°C operating temperature ranges, while K and T grades of the ADSP-1009 specify 155 ns and 180 ns cycle times for the same temperature ranges.

All models are available in a 64-pin hermetically sealed ceramic DIP, 68-pin pin-grid array (PGA), or a 68-terminal leadless chip-carrier. Other features include operation with a single +5-V power supply, TTL-compatibility, and diode-protected inputs. Prices start at $80 for the ADSP-1012 and $95 for the ADSP-1009.

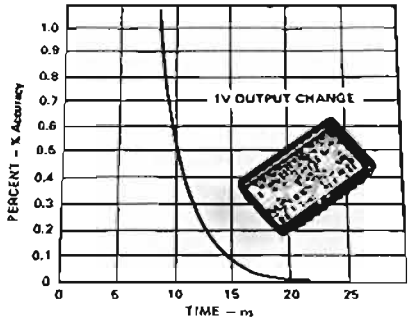
Fastest Acquisition Time of 14 ns typ, 19 max, to 0.1%

Hybrid HTS-0010 Supports Sample Rates to 100MHz

The HTS-0010* is the industry's fastest track-and-hold amplifier, with its 14-ns typical, 19-ns maximum acquisition time and 5 ps maximum aperture jitter (uncertainty), fostering accuracy in circuits that process high-speed real-world signals.

Other key features include slewing rate of 300 V/μs, 40-MHz minimum full-power bandwidth, and 60 MHz minimum small-signal bandwidth, as well as a maximum droop rate of only ±0.1mV/μs. Its output current of ±40 mA easily drives capacitive loads and low input impedances typical of flash and fast successive-approximation ADCs.

Such high performance suggests use ahead of flash encoders in data-acquisition applications, where fast ac signals are sampled and digitized at up to 100 MHz. It can also deglitch the output of fast d/a converters, by holding its output constant during switching transients in the DAC's output, an important consideration in function generation



and display graphics (glitches can cause substantial discontinuities in analog functions and irregularities in displayed images).

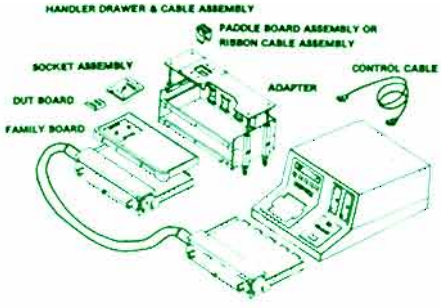
The HTS-0010 can also be used in radar and medical electronics, communications equipment, displays, and test equipment. Pin-compatible with the HTS-0025, it simplifies upgrading of existing designs.

Packaged in a 24-pin hermetically sealed metal DIP, it is available for both 0°C to 70°C and −55°C to +125°C (K/S grades). Prices in 100s are $315/$368.

New Product Briefs

TEST BOARDS

For Fast MCT-Handler-Based Tests of Digital Devices



The MCT Handler Interface Boards* are designed for easy adaptation of LTS-2000 Series benchtop automatic device testers to automatic component-handler testing of SSI and MSI digital devices. Fully compatible with, and prewired for, MCT (Microcomponent Technology) 2600 and 3600 Series handlers, these boards enable accurate tests to be performed at high speed. The same test programs used for manual testing are used for testing at the handler site, easing the test engineer's burden.

An interface board set consists of an MCT DUT (device-under-test) Board and an MCT Paddle-Board assembly. The DUT boards are already wired for the standard pinout configurations found in digital ICs; this means that the test engineer does not have to spend time configuring the board for standard TTL and CMOS devices.

The DUT Boards and the Paddle-Board Assemblies are constructed with a third layer of circuitry devoted entirely to a ground plane. The ground plane provides a very low-impedance device ground and provides tight ac decoupling of the device pins. This results in quite low noise levels during tests.

Six DUT boards are available, wired for standard device-package configurations with 14 to 24 pins. On these boards, the pin with the highest number is wired to V_{CC}, the pin with half that number is wired to Ground; all other device pins are connected to pin-driver/detectors (see "Test Digital and Linear ICs with LTS-2000 Test Systems," *Analog Dialogue* 17-1: (20-21). Provisions are made for devices with nonstandard pinouts and for special circuitry.

*Use the reply card for technical data.

INDUCTOSYN/RESOLVER-DIGITAL CONVERTER

Hybrid IRDC1732 Has Lowest Cost – from $89 (100s) Tracks at 100 Pitches or Revolutions per Second

The IRDC1732* converts resolver-format (sine and cosine) signals into a 12-bit parallel digital word. If the inputs come from a resolver, the output represents the angle of the resolver's shaft; if the inputs are from an Inductosyn™ slider, the output word represents the fractional position of the slider within an Inductosyn pitch.

Converting linear or angular positional information into parallel digital format, the IRDC1732 has latchable 3-state output registers for microprocessor interfacing. The device's 12-bit resolution, 100-revolution (or -pitch) per second tracking rate, and compact packaging make it suitable for industrial and machine-tool control, robotics applications, and (in the hermetically sealed metal-packaged version designed for −55°C to +125°C operating temperatures) military requirements.

Accuracy is specified in terms of ±21 arc-minute maximum error. There are two signal/reference-frequency options—400 Hz and 1 kHz-to-10 kHz. For the 400-Hz version, the minimum tracking rate is 50 revolutions (or pitches) per second.

The IRDC-1732 requires a +5-V logic supply and a dual power supply, which may range from ±12V to ±15V. Two choices of 32-pin DIP package are offered: ceramic (0°C to +70°C) or the hermetically sealed metal case. Pricing in 100s starts at $89 for the commercial grade.

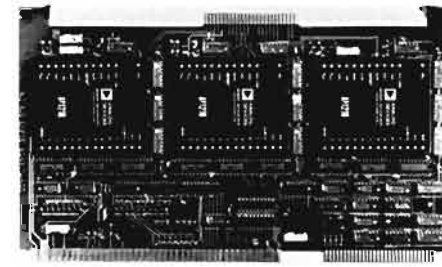
µP-CONTROLLED 3-AXIS CONVERSION

MCI-1794: A 3-Channel MULTIBUS-Compatible Board For Inductosyn/Resolver-to-12-Bit Conversion

The MCI-1794* is a three-channel 6.75″ × 12″ (172 mm × 305 mm) MULTIBUS™-compatible board that converts resolver or Inductosyn™ signals to 12-bit digital data for applications in computer- and numerically controlled machines. It is compatible, both electrically and mechanically, with Intel 8080-, 8085-, and 8086-based systems and operates from standard MULTIBUS power supplies.

The MCI-1794 greatly simplifies the interfacing of position information to computers in industrial applications, such as machine-tool control, robotics, drafting machines, and plotters. The multi-channel converter interfaces directly with 8- or 16-bit buses and interfaces with processors as either I/O (input/output) or memory.

Using continuous Type II tracking conversion, it provides a minimum tracking rate of 10,200 pitches (Inductosyn) or revolutions (resolver) per minute. A 12-bit pitch counter, which advances 1 bit on each full-scale carry—i.e., each 360° of rotation or each pitch, provides up to 24-bit maximum angular resolution.



Each channel is transformer-isolated (500 V dc) and provides a dc output voltage proportional to angular velocity for rate (tachometer) feedback. Reference-signal frequency options are 400 Hz, 2.6 kHz, 5 kHz, and 10 kHz. Price starts at $1000 (1's).

™Inductosyn is a registered trademark of Farrand Industries, Inc.

MULTIBUS is a registered trademark of Intel Corporation.

MORE AUTHORS *(continued from page 2)*

Steve Kirby (page 19) is a Project Engineer at Analog Devices, Ltd., East Molesey, Surrey, England, working on synchro-digital converters. Graduated from Sussex University (B. Sc. in Electronic Engineering), he is now in the final throes of his Ph.D. candidacy at York University, where he has also worked on electronics projects for local industry at York Electronics Center. He designed the Cryometer 100K while at YEC. His Ph.D. research was on a carrier-domain magnetometer (invented by ADI's Barrie Gilbert). He has also worked in medical electronics at Cardiac Recorders, Ltd. His outside interests include walking, geology, woodworking, and—electronics.

Chuck Kitchin (page 11) is an Associate Engineer at Analog Devices Semiconductor. For the past eight years, he has designed IC applications circuits and assisted in product development at ADS. Holder of an ASEE from Wentworth Institute, and now attending the University of Lowell, he previously worked for Kybe Corp. and radio stations WMEX and WCRB (Boston). Chuck's leisure activities include jogging, astronomy, and wine tasting.

Doug Mercer (page 24) is a Design Engineer at Analog Devices Semiconductor. He was graduated from Rensselaer Polytechnic Institute with a BSEE in 1977 and joined ADS as a Production Engineer, moving into Design in 1979. In addition to designing the AD670 and the AD567 DAC, Doug is co-inventor and designer of the AD558 DACPORT™; he co-authored a talk on it at the IEEE International Solid-State Circuits Conference and later co-authored a paper on it in the IEEE *Transactions on Solid-State Circuits.*

Al Ryan (page 3), Senior Staff Engineer for ADI's Component Test Systems Division (CTS), has a BSEE from the University of Massachusetts at Amherst. He joined Analog Devices ten years ago as Test Engineer for the Semiconductor Division. He was responsible for developing the system concepts and designing much of the hardware of ADI's highly successful LTS-2000 family of benchtop testers. He is now working on the next generation.

(More authors will be found on page 30.)

ADI Division Fellow Named

Lewis Counts

Lew Counts, Engineering Manager for Linear Products, has been named a Division Fellow at Analog Devices Semiconductor (ADS), in recognition of his contributions to both the formulation and implementation of linear product strategy. He was also appointed to the Division Staff by Jerald Fishman — Group Vice President and acting General Manager of ADS.

For the past 13 years, Lew has designed many successful linear products at Analog Devices, including op amps, log-antilog circuits, multipliers, dividers, multifunction components, and rms-to-dc converters. Eight years ago, he made the transition from discrete design at our Modular Instrumentation Division to IC design at ADS; one of his most recent products, the AD637 rms-to-dc IC, is discussed on pages 11-13 of this issue.

The word "designed" is inadequate. We really mean that, as an advocate, he foresaw the need for, proposed, twisted arms, designed, introduced, applied, publicized, and—within a fairly short time—demonstrated the outstanding success of such products as IC rms-to-dc converters and high-precision bipolar-FET op amps.

As a communicator, Lew has been a frequent contributor to these pages, a major contributor to the Analog Devices *Nonlinear Circuits Handbook*, author of articles appearing in leading technical magazines, and a participant—as a recognized leader in the industry and IEEE Member—in seminars and conferences, most notably the IEEE International Solid-State Circuits Conference.

As leader and mentor, he was able to recruit a strong linear design team, has contributed to their development, and has ensured that their creative talents are productively employed.

Combining all of these accomplishments and capabilities with an eager participation in constructive solutions to daily problems, he has emerged as a clear technological leader at ADS. Because Lew is a technical leader, an individual contributor, and a key member of the ADS staff, he has been appointed as a Division Fellow.

Lew is a graduate of the Massachusetts Institute of Technology. He lives in Lexington, Mass., with his wife, Connee, and two daughters. He enjoys cross-country skiing and photography.

Division Fellow is one of the highest levels of technical advancement within the divisions of Analog Devices.

Fellows are recognized for their innovativeness and outstanding technical contributions to the company, for acting as mentors to young technologists, for having demonstrated leadership of outstanding technical groups or in generating new business opportunities, and for having developed valuable industry and academic relationships for the company.

Lew is our fifth Division Fellow. He joins the select company of A. Paul Brokaw (1979), Barrie Gilbert (1979), Jack Memishian (1980), and Mike Timko (1982). ◘

Worth Reading

NEW PUBLICATIONS FROM ANALOG DEVICES

RMS-to-DC Conversion Application Guide

This free 46-page booklet, by Charles Kitchin and Lew Counts (see pages 11-13 and 29), will tell you everything you need to know—and much more besides—about rms-to-dc conversion. Profusely illustrated, with 75 Figures and 5 Tables, it is divided into 3 main sections: RMS-DC Conversion Theory (including definitions, methods, and principles of device operation), Basic Design Considerations (including accuracy, filters, averaging, settling time, crest factor, single-supply operation, dB outputs), and more than a dozen Application Circuits. In addition, there are three useful appendixes: Testing the Critical Parameters of RMS Converters, Input Buffer Amplifier Requirements, and Computer Programs for errors, ripple, and settling time. Use the reply card to request a copy.

High-Speed Data Conversion is a free 10-page short-form guide to our line of video and other high-speed data converters. It includes tabular information on High-Speed ADCs, High-Speed DACs, Video ADCs with Track-and-Hold, Communications Converters, Display DACs, and high-speed Multiplying DACs. Also included are High-Speed Instrument Converters and High-Speed Signal Conditioning (Track-Hold Amplifiers, Op Amps, and Buffer Amplifiers). Use the reply card to request your free copy.

Write in on your letterhead for a copy of the latest **LTS-2000 Series Test Systems Product Catalog** from our Component Test Systems Division.

BIBLIOGRAPHY ON RANDOM NOISE*

Compiled by L. DeVito.

Bennett, W. R. *Electrical Noise.* New York: McGraw-Hill, 1960.

Electrical Noise: Fundamentals & Sources. Edited by Madhu S. Gupta. New York: IEEE Press, 1977. Collection of reprints. Includes the following papers of especial relevance:

Burgess, R. E. "Electronic Fluctuations in Semiconductors." *British Journal of Applied Physics* 6 (June 1955): 185-190.

Oliver, B. M. "Thermal and Quantum Noise." *Proceedings IEEE* 53 (May 1965): 436-454.

Pierce, J. R. "Physical Sources of Noise." *Proceedings IRE* 44 (May 1956): 601-608.

Ragazzini, J. R. and Chang, S. S. L. "Noise and Random Processes." *Proceedings IRE* 50 (May 1962): 1146-1151.

van Vliet, K. M. "Noise in Semiconductors and Photoconductors." *Proceedings IRE* 46 (June 1958): 1004-1018.

Freeman, J. J. *Principles of Noise.* New York: John Wiley & Sons, Inc., 1958.

Motchenbacher, C. D., and Fitchen, F. C., *Low-Noise Electronic Design.* New York: John Wiley & Sons, Inc., 1973.

Robinson, F. N. H. *Noise in Electrical Circuits.* Oxford University Press, 1962.

van der Ziel, A. *Noise.* Englewood Cliffs, N.J.: Prentice Hall, Inc., 1954.

Noise in Bipolar Junction Transistors

Nielsen, E. G. "Behavior of Noise Figure in Junction Transistors." *Proceedings IRE* 45 (July 1957): 957-963.

Stewart, J. M. "The Noise Figure of Junction Transistors." *Proceedings IEE* (May 1959, Part B, Supplement No. 17): 1056-1066.

van der Ziel, A. "Noise in Junction Transistors." *Proceedings IRE* 46 (June 1958): 1019-1038.

van der Ziel, A. "Theory of Shot Noise in Junction Diodes and Junction Transistors." *Proceedings IRE* 43 (Nov 1955): 1639-1646.

Noise in MOS and JFET Transistors

Hsu, S. T. "Surface-State Related 1/f Noise in MOS Transistors." *Solid State Electronics* 13 (1970): 1451-1459.

Jordan, A. G., and Jordan, N. A. "Theory of Noise in Metal-Oxide Semiconductor Devices." *IEEE Transactions on Electron Devices* ED-12 (March 1965): 148-156.

Klaasen, F. M. "On the Geometrical Dependence of 1/f Noise in MOS Transistors." *Phillips Research Reports* 25 (1970): 171-174

Mukunda B. Das. "FET Noise Sources and their Effects on Amplifier Performance at Low Frequencies." *IEEE Transactions on Electron Devices* ED-19 (March 1972): 338-348

Shu-Yau Wu "Theory of Generation-Recombination Noise in MOS Transistors." *Solid-State Electronics* 11 (1968): 25-32

MORE AUTHORS *(continued from pages 2 and 29)*

Tim Scranton (page 3), an Applications Engineer at ADI's Component Test Systems Division, recently presented a paper on noise testing at ATE-East, 1983. He has a BSEE from Rochester Institute of Technology and is working toward an MBA at Northeastern University. Before joining ADI, Tim worked as a design engineer for GTE-Sylvania, developing baseband and microwave communications systems. He is a member of Tau Beta Pi; his outside interests include music, dancing, and theatre.

Hans Tucholski (page 22) is a Senior Design Engineer at Analog Devices B.V., Ireland. A native of Lüdenscheid, W. Germany, he was graduated in 1968 and holds a Dipl. Ing. (grad) für Electroteknik. Before joining AD-BV, in 1976, he was with DEC in Galway, Ireland, Technical Manager of a color-TV startup venture in Dublin, and Color-TV Design Engineer with Blaupunktwerke GmbH (Boschgroup) in W. Germany. He has a patent and several publications.

John Wynne (page 22) is an Applications Engineer at Analog Devices B.V. (Limerick, Ireland). Previously he was Telecommunications Project Engineer in the City of Dublin Devin Street Technical College, and later a Design Engineer at Sperry Gyroscope Avionics Division U.K.

*None of the publications listed in this bibliography are available from ADI.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE . . . (Volume 17, Number 3, 1983 -- 28 pages):

Basic-Programmable Single-Board Measurement & Control System (uMAC-5000)
Program Interrupts, Error Trapping, Program Workspaces - Advanced Features of uMACBASIC Real-Time Measurement-and-Control Programming Language
12-Channel Expander Board for uMAC Systems (uMAC-4015)
MUX200 Increases Channel Capacity of MACSYM 350 Systems
Data-Acquisition information System (DAiS) - Menu-Driven Monitoring System with MACSYM 150 and 350
Booleans, 8-Color Plotter, 10-MB Winchester Buffers - MACBASIC 3 Enhancements for MACSYM
Ground Rules for High-Speed Circuits
New-Product Briefs:
- IC RMS-to-DC Converter with Highest Accuracy and Widest Bandwidth (AD637 - also page 11, this isue)
- IC Instrumentation Amplifier with Lowest Offset Drift and Noise (AD624)
- IC Amplifier/Compensator for Type K Thermocouples (AD595)
- uP-Compatible 12-Bit IC Multiplying DACs for 8-Bit Buses (AD7548)
- IC Low-Cost Complete uP-Compatible 8-Bit (15-us) A/D Converter (AD673)
- uP-Compatible IC 10-Bit ADC: No Missing Codes over Temperature (AD7573)

Book Review: Electrostatic Discharge Control - Successful Methods for Microelectronics Design and Manufacturing (not available from Analog Devices)
Editor's Notes, Authors, New Publication, Potpourri, Advertisement.

NEWS FROM ROME - MIL-M-38510 ELECTRICAL CHARACTERIZATION . . . According to the July, 1983 RAC Newsletter (published by Reliability Analysis Center, a DoD Information Analysis Center operated by IIT Research Institute, Chicage) a number of IC and hybrid parts available from Analog Devices, either as originator or generically, have been electrically characterized and appear on MIL-M-38510 "slash" sheets. Devices listed were: (a) ADI parts: (AD)565 & (AD)566 12-bit DACs (/12103, /04); AD571 10-bit ADC (/134); (AD)2700 & (AD)2702 hybrid 10-volt references (/136); (b) generic parts: OP07 & OP27 low-noise precision op amps (/135); DAC87 12-bit DAC, hybrid & monolithic (/137) . . . Characterization is also near completion on: AD574 12-bit ADC, 346 fast sample-hold, and VFC32 V/F converter.

DATA-SHEET ERRATA . . . AD9768 DAC: in Figure 4, pins 15 and 16 should be externally wired together . . . HOS-050 and HOS-060 data sheets: the Note under the Pin Designations table and/or under the Outline and Pin Designations information should read: *Pins for connecting optional offset potentiometer. Recommended value is 10 k ohms, with center arm connected to +15 V.

OUR FACES ARE RED DEPARTMENT . . . In the article, "Avoiding Passive-Component Pitfalls" (Analog Dialogue 17-2), Figure 6 and its context suggest that "heat ... rises." What actually rises is heated air, but what forms the temperature gradient, when the resistor itself has little dissipation, is the difference between the temperatures of the lead attached very close to a hot board and the longer lead that may be relatively cooled by moving air. If the resistor has substantial dissipation, the difference between the more rapid heat transfer via the short lead and the slower heat transfer to the air and via the long lead will produce a gradient; in this case, however, the resistor's tempco will probably be the dominant source of error. Our thanks to Professor D. B. Brumm, of Michigan Technological University, for calling our attention to this lapse, giving us an opportunity to set the record straight.

PATENTS . . . 4,400,689 and 4,400,690, to A. Paul Brokaw and Modesto A. Maidique for "A-to-D Converter of the Successive-Approximation Type," i.e., the AD571 . . . 4,399,345 to Jerome F. Lapham and Tommy D. Clark for "Laser Trimming of Circuit Elements on Semiconductive Substrates."

PRODUCT NOTES . . . 3B Series: the AC1350 Blank Module is available, permitting users to create their own functions in packaging compatible with the 3B series of standard modular signal-conditioning components. The module consists of a 3B Series case, blank labels for user markings, and a 3B Series breadboard. It is also available without the breadboard . . . MACSYM 150 and 200 are available for a variety of power supplies. Get in touch with ADI System Sales for information . . . AD561, the low-cost monolithic 10-bit DAC, is now priced even lower in its plastic AD561JN and AD561KN versions. $10.90 and $18.10 in 100s.

The AD539. A 60 MHz analog multiplier for under $15.

Analog has redefined high-speed analog signal processing—right up to an incredible 60 MHz—with a new IC: the AD539.

This versatile, dual-channel, analog multiplier provides excellent AC characteristics up to and beyond video frequencies.

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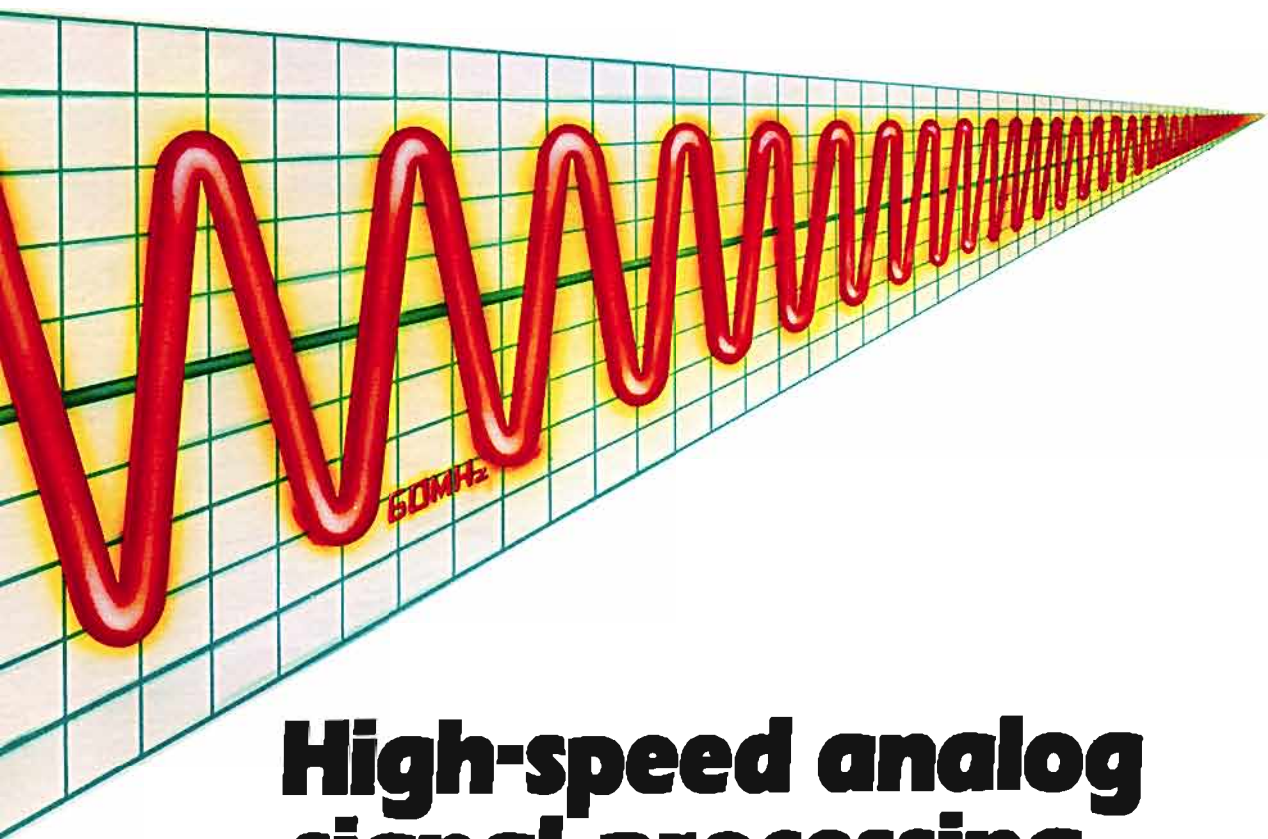
The AD539's great versatility and performance capabilities make such applications possible. Two independent, low-distortion signal channels handle bandwidths up to 60 MHz. A common control channel provides linear control of gain up to 5 MHz. Differential phase linearity—which is critical in video applications—is less than ±0.2° at 3.58 MHz. At the same time, the use of an internal bandgap reference and laser-trimmed thin-film resistors maintains excellent DC performance.

To let you see for yourself just how fast and versatile the AD539 can be, we're offering a demo board. It has all the proper grounding and decoupling to assure maximum performance in either voltage or current-out modes. Ready for you to add the power supply and input signals.

For more information on the AD539 High-Speed Analog Multiplier, contact Steve Miller.

ANALOG DEVICES



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